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DDS Based Harmonic Signal Generator

Dr.G.S.K.Gayatri Devi[1], Dr.J.Shirisha[2]
Professor[1], Associate Professor[2]
Department of ECE
Malla Reddy Engineering College

Abstract*:* In order to create this harmonic signal generator, direct digital frequency synthesis (DDS) technology was used in its development. The basic DDS structure is presented, and a kind of compression ROM is devised as a result of this. The DDS core with compression ROM is then built using the Xilinx Xc3s500e fpga and the VHDL language on the Xilinx Xc3s500e fpga. In particular, performance characteristics like as integration and expansibility have been significantly enhanced. Specifically, the article discusses the DDS core idea, and it presents an efficient structure for the DDS core. Overall, the gadget used 0.081W of electricity, according to the researchers.

Key Words*:* DDS, SOPC, harmonic signal generator, Noise

I. INTRODUCTION

A signal generator is finding more and more uses in current industrial detection and communication systems and equipment. Particularly popular is the harmonic signal generator, which allows for fine tuning of the frequency and phase. Aside from that, in certain particular situations such as the power system, the harmonic proportion control, multi-channels, and mixing-frequency sine wave output are all required. The DDS technology is the foundation of the majority of signal generators now on the market. Tierney, Rader, and Gold [1] introduced the DDS technique to the world in 1971 [1. It is a kind of frequency synthesis technology in which the waveform is directly synthesised on the basis of the phase of the signal. Tierney, Rader, and Gold are also credited with introducing the traditional framework in 1971. With the advancement of microelectronic technology, more and more single channel DDS chips are being produced by chip suppliers such as analogue device Inc. and other similar companies. The DDS is highly favoured in several contemporary communication and detection systems because to its many benefits, including quick switching, precise frequency resolution, minimal phase noise, and continuous-phase frequency switching, among other things. One severe issue, however, is the limited functionality of single channel DDS devices.The distance between chips is minimised, and the overall performance and functionality of the system are greatly enhanced. With the advancement of Field FPGA chips, it is becoming feasible to include the

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CPU inside FPGA chips. Xilinx Inc. and Xilinx Inc. are the companies that provide the System on a Programmable Chip solution (SOPC). SOPC is an on-chip reconfigurable system that is based on the FPGA technology. It is a holonomic system that incorporates a processor, a memorizer, I/O ports, and other essential components into a system that is intended for the realisation of certain logic operations. In part, this is due to the fact that SOPC is a versatile and effective SOC solution due to its flexibility in system design, reduction, extension, upgrading, and so on. Its hardware and software systems, in addition, may be customised [2]. As a result, when a signal generator is developed to tackle a control issue, the SOPC concept might be used to solve the problem. In this study, we present the design of a signal generator with configurable frequency, phase, and harmonic proportion. It is necessary to employ an FPGA chip in order to actualize the DDS logic and other modules. [3] A kind of soft core Nois II is placed on an FPGA chip, allowing the system to be operated more flexibly. In addition, several simple circuits are constructed to ensure that the output signals are steady and clean.

II. PRINCIPLE OF DDS SYNTHESIS

Digital frequency synthesis is a novel frequency synthesis method that directly synthesises waveforms on the basis of phase, as opposed to analogue frequency synthesis. In accordance with the connection between phase and amplitude, the phase of the waveform is segmented and allocated to the appropriate addresses [4]. Among the many benefits of DDS technology are its speed, precise frequency resolution, minimal phase noise, continuous-phase frequency switching, and so on. The DDS idea is straightforward to comprehend. To begin, a single frequency sine signal should be sampled for one period in accordance with the Shannon Sampling Theorem, and the results should be recorded. It is expected that we sample N 2 points in one period of a sine signal and then store the points in a ROM with N 2 addresses, as shown in the diagram. The preceding course's sequence is converted into our own. The data contained in the ROM is read out first, followed by the rest of the data.

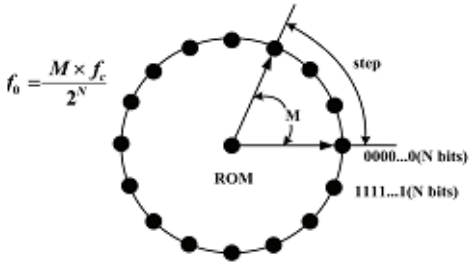

Fig 1. Principle of the DDS.

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The Numerically Controlled Oscillator (NCO), Digital to Analog Converter, and Filter are the components of the DDS's traditional function Object() { [native code] }. Figure 2 depicts the situation. The NCO is responsible for storing the phase accumulator and the ROM lookup table. It is the foundation of DDS. With frequency control word M (N-bit) in each clock period, the output of phase accumulator is collected, and the high L-bit results of the output are utilised as address input to the ROM lookup table. The fundamental wave, the third harmonic, and the fifth harmonic are all present. Besides being able to modify the frequency and phase of the fundamental wave, the percentage of every single frequency harmonic in a mixing-frequency signal may also be adjusted using this technique. This device's frequency should be adjustable from 1kHz to1MHz with a resolution of 10Hz, its phase should be adjustable from 0o to 360o with a resolution of 1o, and its harmonic proportion should be adjustable from 0 to 40% with a resolution of 1 percent, according to the specifications listed below. The output signals are typically two channels of 100 kHz sine waves with a 180o phase difference between them.

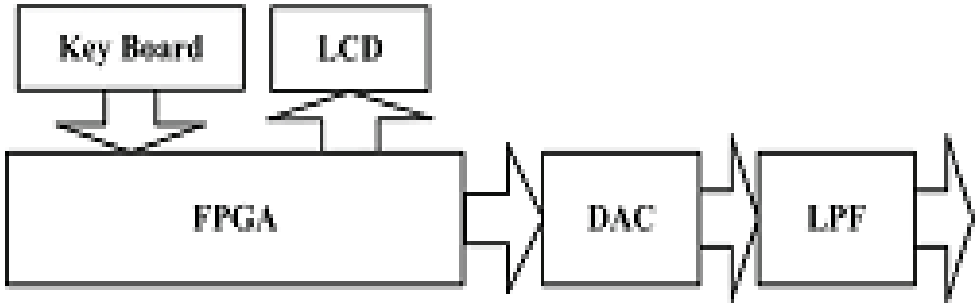
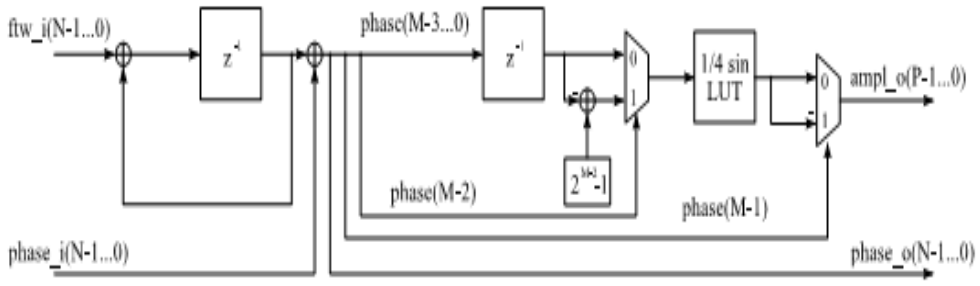


Fig 3. Block diagram of system.

IV. IMPLEMENTATION RESULTS



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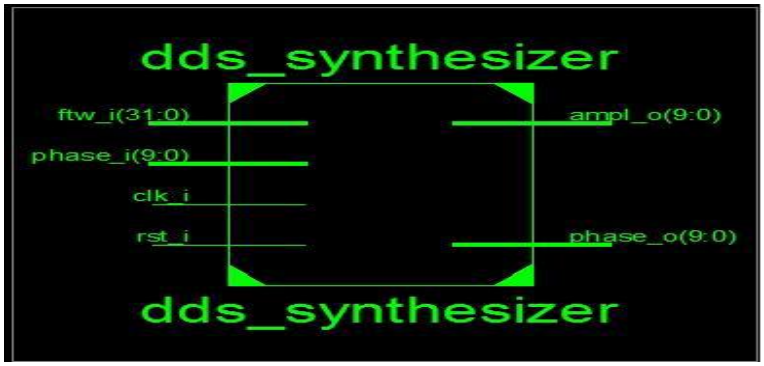

Block diagram of the DDS Implementation

Conclusion

The basic DDS structure is presented, and a kind of compression ROM is devised as a result of this. The DDS core with compression ROM is then built using the Xilinx Xc3s500e fpga and the VHDL language on the Xilinx Xc3s500e fpga. In particular, performance characteristics like as integration and expansibility have been significantly enhanced. Specifically, the article discusses the DDS core idea, and it presents an efficient structure for the DDS core.

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