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DESIGN OF HIGH SPEED AND AREA EFFICIENT HYBRID HANCARLSON ADDER USING PRPG

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ABSTRACT: In this paper design of high speed and area efficient hybrid HanCarlson adder using PRPG is implemented. Basically, adders plays very important role in DSP and micro processor applications. Input 'A' and input 'B' are the inputs given to carry mask able half block. Propagator and generator unit generate the signals of propagator and generator. Hybrid Han Carlson Carry generation unit will generate the carry. At last output is obtained. PRPG is used to produce vectors to test the circuit. From results it can observe the RTL schematic, Technology schematic of configurable parallel adder. Hence the hybrid Han Carlson adder gives effective results.

KEY WORDS: Approximate computing; Carry Mask able Adder, Hybrid Han Carlson Carry generation unit.

I. INTRODUCTION

Fastest technologies are developed in present days. In present days, reduction of device size, fast operation and low power consumption are required. The designing of low power VLSI system has more demand in mobile communication. Due to the device designed by designer with high speed, low power consumption and small silicon area, the device is available with low power. ALU (Arithmetic logic unit) and FU (Floating point unit) are the main parts in computations [1]. Logical computations are addition, subtraction, multiplication, division and logical operations are AND, OR, INV and comparison which are processed by Arithmetic logic unit (ALU). Data path has an important role in digital signal processors and microprocessors because of some characteristics such as power consumption, speed of operation and die-area.

The above characteristics depend upon the data path efficiency. Data path contains complex operations are subtraction, addition, division and multiplication [2].

The main important factor is data path performance which is affected by efficient hardware units of complex computations. In the data path addition is the important executed operation, addition operation contains binary adder to add given numbers. In complex computations such as decimal operations, multiplication and division, adders has important task [3]. To get data path efficiently, the implementation of binary adder should be efficient.

In central processing unit (CPU) crucial element is ALU (Arithmetic logic unit). An adder has important function in ALU and an adder performs not only addition but also performs multiplication, subtraction and decrement/increment. In ALU and general processors to get better performance, efficient adder is needed. From 1950s, for

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hardware implementation of VLSI arithmetic circuits, research started on efficient adder implementation. In control systems and digital signal processing main operation is the addition.

The properties of system or processor like accuracy and speed depends upon the performance of adder. To execute the addition of numbers, adder is used which is a digital circuit. Different processors and computers contains ALU in which adder is used. To reduce different parameters, different designs have been implemented based on parallel and serial structures. Four elementary operations are performed in binary addition.

The adders can be represented in many forms like BCD (binary coded decimal) and excess-3 code; binary numbers are used in adders to perform the operation. Negative numbers are represented by ones complement or two's complement, for this adder is modified as adder-subtractor. More logic is required to represent signed numbers including basic adder [4-5].

To execute the addition operation, computers contain Arithmetic Logic unit (ALU) in which adders are mostly used. Graphics processing unit (GPU) and central processing unit uses the adders to decrease the redundancy for the graphics applications. In the adders first type is half adder it include two inputs and it provides two outputs such as carry and sum. Next one is full adders which include two inputs with carry input and it provides two outputs such as carry and sum. For single bit, both half adder and full adder is utilized. The full adder is coupled in parallel form to perform the multi bit addition operation.

II. RELATED WORK

Half adder is used in digital electronics for the purpose of addition of two binary numbers. Full adder is used for the addition of 3-bit input sequence. If input sequence contain more number of bits, half adder and full adder does not satisfy the addition

operation. These drawbacks are overcome by Ripple carry adder. For the addition of N-bit numbers, this type of logic circuit is used in digital operations.

By using multiple full adders, logical circuit can be created for the purpose of addition of N-bit numbers. In each full adder, one of the sources of info is Cin which is taken care of from Cout of past adder. This kind of adderis known as Ripple-Carry Adder. Since each convey bit waves to next full adder. May be half adder is put in the principal full adder since first full adder contains Cin=0.

The Ripple convey adder circuit chart is straightforward, it creates quick plan time. In any case, the activity of wave convey adder is moderate on the grounds that each full adder ought to be hanging tight for convey bit which is originated from past full adder. By utilizing full adder circuit, door postponement can be determined. Three degrees of rationale are required in full adder. N full adders are required in n-bit Ripple convey adder.

BCD (binary coded decimal) adder is a digital circuit in which two BCD numbers are added in parallel and carry out and sum bits are generated. The result of sum will not be in BCD form when addition of two BCD digits is done.

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The BCD result is correct in first example and BCD result is not correct in second example. BCD digits are represented from 0 to 9, to represent BCD numbers, four bits are required. But by using four bits, 16 values are represented. In the BCD digits extra six values are ignored because BCD digits are represented from 0 to 9. After addition, the result will not in BCD form

when the result is greater than 9. It contains corrections to be done to obtain correct BCD results

III. EXISTED SYSTEM

The above figure (1) shows the architecture of existed system. The existed framework structured a precision configurable adder by concealing the carry proliferation at runtime. This adder accomplishes the first reason for carrying a fair-minded advanced outcome among force and deferral without giving up precision. Furthermore, because of the modest number of transistors, the CMHA profits by generally short wiring lengths just as a customary and basic format.

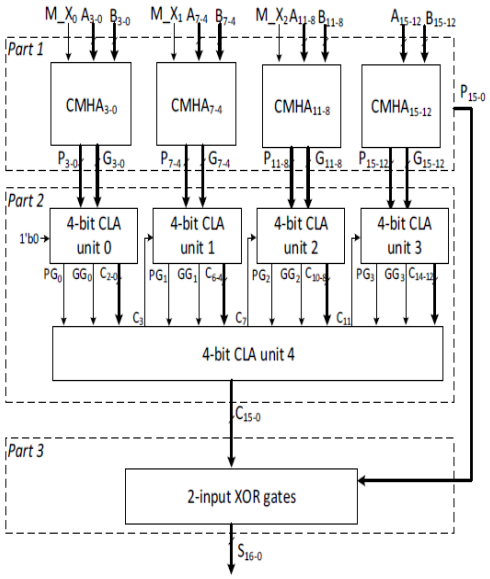

Fig. 1: EXISTED SYSTEM

The similarly lower speed of this adder structure, in any case, restricts its utilization for rapid applications. In this paper, given the alluring highlights of the CMHA structure, we have concentrated on diminishing its deferral by adjusting its execution dependent on the static CMHA rationale. The fixation on the static CMOS starts from the craving to have a dependably working circuit under a wide scope of gracefully voltages in exceptionally scaled innovations.

The existed alteration speeds up significantly while keeping up the low zone and force utilization highlights of the CMHA. Furthermore, an alteration of the structure, in light of the variable idleness procedure, which thus brings down the force utilization without significantly affecting the CMHA speed, is additionally introduced. As far as we could possibly know, no work focusing on plan of CMHAs working from the super edge district down to approach limit area and furthermore, the structure of (half breed) variable inertness CMHA structures have been accounted for in the writing.

IV. PROPOSED SYSTEM

The below figure (2) shows the block diagram of proposed system. Input ‘A’ and input ‘B’ are the inputs given to carry mask able half block. Propagator and generator unit generate the signals of propagator and generator. Hybrid Han Carlson Carry generation unit will generate the carry. At last output is obtained.

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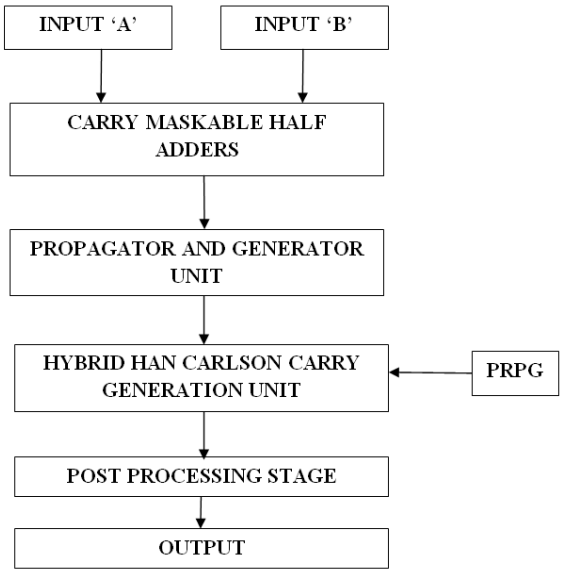

Fig. 2: BLOCK DIAGRAM OF PROPOSED SYSTEM

Propagate signals and generate signals are manipulated to pair of each inputs A and B. In hancarlson adder carry generation stage the calculation is performed based on the bits and carries obtained. The entire operation is performed in the form of parallel. Generate and propagate signals are obtained from the intermediate signals.

Han Carlson adder performs its operation in three stages they are

1. Pre-Processing Stage:

In this stage, propagate signals and generate signals are manipulated to pair of each inputs A and B. Propagate signal and generate signal are represented as

Pi = Ai XOR Bi

Gi = Ai AND Bi

2. Carry Generation Network:

In carry generation stage the calculation is performed based on the bits and carries obtained. The entire operation is performed in the form of parallel. Generate and propagate signals are obtained from the intermediate signals. The below equations shows the propagate and generate signals:

Pi:j = Pi:k AND Pk-1:j

Gi:j = Gi:k OR (Pi:k AND Gk-1:j)

3. Post Processing Stage:

In post processing stage the calculation is performed based on the input bits. From post processing stage sum and carry is generated. The below equations shows the sum and carry equations:

Ci = (Pi AND Cin) OR Gi

Si = Pi XOR Ci-1

In applications of high speed circuits, very useful adder is Kogge-Stone adder. Kogge-Stone adder is designed based on the power and area.

Structure delay= $\log_2 n$

Number of computation nodes= [(n) ($\log_2$ n)-n+1]

V. RESULTS

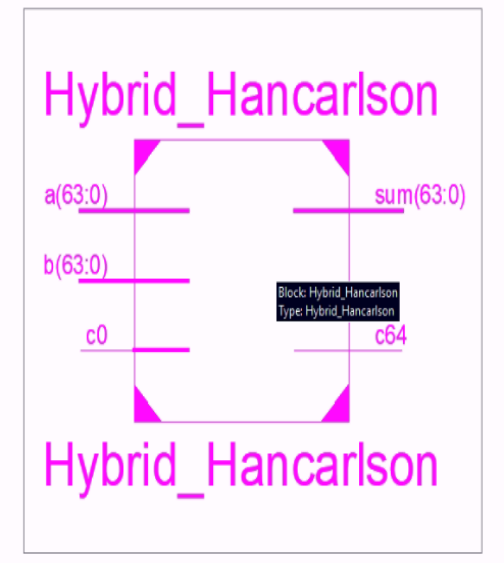

Fig. 3: RTL SCHEMATIC

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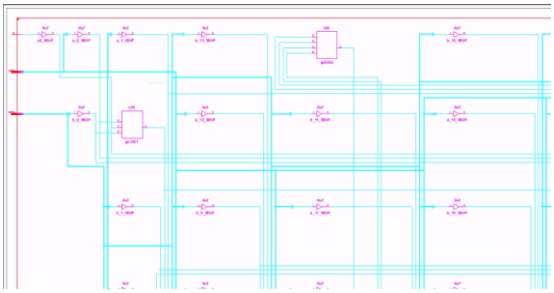

Fig. 4: TECHNOLOGY SCHEMATIC

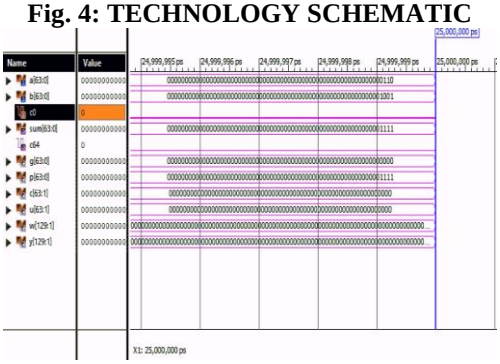

Fig. 5: OUTPUT WAVEFORM

VI. CONCLUSION

Hence in this paper the design of high speed area efficient hybrid HanCarlson adder is implemented. Propagator and generator unit generate the signals of propagator and generator. From results it can observe the RTL schematic, Technology schematic of configurable parallel adder.

VII. REFERENCES

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