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LOW-POWER RETENTIVE TRUE SINGLE-PHASE-CLOCKED FLIP-FLOP WITH REDUNDANT-PRECHARGE-FREE OPERATION

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ABSTRACT:

In complementary metal oxide semiconductor circuit based designs, gates and flip-flops are essential part of the clocking circuits. They are responsible for the synchronous-asynchronous behavior to the system. The basic circuit of flip flop which are modelled with XOR or XNOR and are used in various digital circuits determines the system power consumption. The type of flip flop used in digital circuits determines the output load of the circuits. This is also known as clock load. This clock load directly affects the switching power consumption of circuits. Therefore, it is essential to introduce one technique to minimize the power consumption of flip flops to reduce the overall system power consumption. The power specification of modern portable digital circuits is severely limited. It is very essential to improve system power performance in the flip flop networks. Timing elements like flip-flops are very important for the performance of digital systems. This is due to the extremely large set up time and hold time. These are also essential for good performance and better efficiency. Our design aims to initiate a low power design with 4 bit proposed PAFL D-FF and 1 bit T-FF ensuring the correct design parameters. These parametric criteria would suggest the design of the Flip flop would be based on the clock gating procedure to reduce the power associated with 1 bit flip flop ensuring the reduced power in multiple bits. Our design improves more than 30% of power reduction when compared to existing design.

Keywords: XOR, XNOR, PAFL D-FF, T-FF.

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1. INTRODUCTION:

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858) while working for Fairchild Semiconductor. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (COS-MOS).[1] The words "complementary-symmetry" refer to the typical design style with CMOS using complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.[2] Two important characteristics of CMOS devices are high noise immunity and low static power consumption.[3] Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or N-type metal-oxide-semiconductor logic (NMOS) logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in very-large-scale integration (VLSI) chips.

The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and smaller sizes.

EXISITNG DESIGN AND PROCEDURE

Many researcher’s interest in the development of a technically acceptable low power VLSI design methodologies have demanded for an ultralow power system that are being attracted as compared to a traditional strategy, which

is been forecasted very recently [3]. With the present generation of devices are from the frequency of fundamental physical limits, for processing a new generation are being developed. Thus, needs for a VLSI chips with low power has raised from such evolution an integrated circuit were forced. In 1971, the Intel 4004microprocessor was developed and had transistors count of2300, that in turn about a 1watt of power dissipated with1MHz frequency. After that a Pentium came in 2001, which had a42 million number of transistors, which dissipated65watts of power with 2.4GHz frequency. A few years later, the microprocessor designed also will have the same power as that of a nuclear reactor, if the power densities rise an exponential way. Such high-power densities introduce the reliability concerns like thermal stress, electro migration and hot carriers induced a device degradation, which would result in the performance loss. Another factor is low power chips which in-turn needs fuel is of increased market demand in all the portable consumer electronics device which are powered through batteries. For the low power requirements, craving of the smaller with lighter and also the more durable electronic products is necessary. The electronics also dissipates more amount of heat with more power consumption, which in-turn requires more costly cooling solutions like fore.g. Liquid cooling cabinets for desktop computers resulting to a higher overall cost of the device with IC. Thus, a product differentiator in almost all portable devices is the battery life. In the batteries life history, no such similar rapid solidity growth has occurred compared to that of electronic circuits even being the biggest and heaviest component in all the portable systems. The power dissipation is gaining prominence being main source in high performable portable digital batteries systems running on batteries like cellular phones, note-book computers and personal digital (PDA) assistants. These systems are directly related to the performance, which effects the battery longevity with a low power consumption as a prime concern [1].A low power VLSI design has assumed greater importance for an active and rapidly developing field, in these situations. A greater number of transistors per chip with better performance in the development of the MOS technology is increasing, which is a main operating feature for any chip manufacturers [1].

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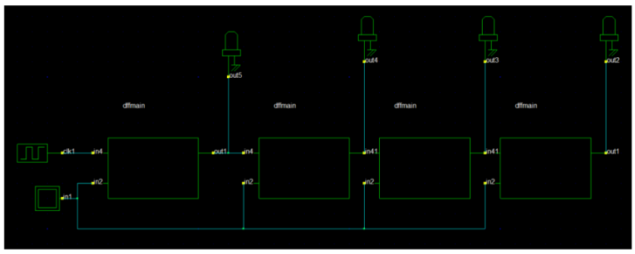
PROPOSED SYSTEM:

POWER minimization has become a primary concern in VLSI design. Several conventional techniques are utilized to curb dynamic and leakage power in conventional CMOS circuits. One of the most effective methods is pipelining and subsequent voltage scaling to minimize energy dissipation at a given operating frequency. At high operating frequencies, however, the energy and delay overhead of pipeline registers becomes significant and degrades overall system efficiency. In systems with significant switching activity, charge recovery circuits have the potential to dissipate less energy than their pipelined, voltage-scaled CMOS counterparts. Several charge-recovery logic styles have been proposed [1]–[5]. Over a range of relatively low operating frequencies (a few hundred megahertz), these charge-recovery techniques have been shown to achieve lower energy dissipation when compared to voltage-scaled CMOS. Achieving energy savings over CMOS at higher operating frequencies has remained elusive, however. Although performance limits of charge-recovery circuits are fundamentally determined by the need for gradually transitioning power-clocks, prevalent operating frequencies in charge-recovery circuits are more a consequence of design than any such fundamental constraint. Some of the main factors that lead to lower speeds in charge-recovery circuits are the use of diode-connected transistors [6], [7], the use of pMOS devices in evaluation trees [8], [9], and the excessive time required to resolve the complementary outputs of the dual-rail gates during evaluation.



Circuit diagram.

The current design on the Flip flop design would imparts the different circuit elements with the gates specifically pmos and nmos which results in estimating the design of each cascaded section of the model represented in the current figure. The design would provide a D-FF condition with 4 bit memory design on each circuit where the current switching of the gates is controlled by the input 2 on the D-flop main. Initially the input is switched on and its customized outputs for each stage is changed with 0000 , 0010, 0100, and 1000.

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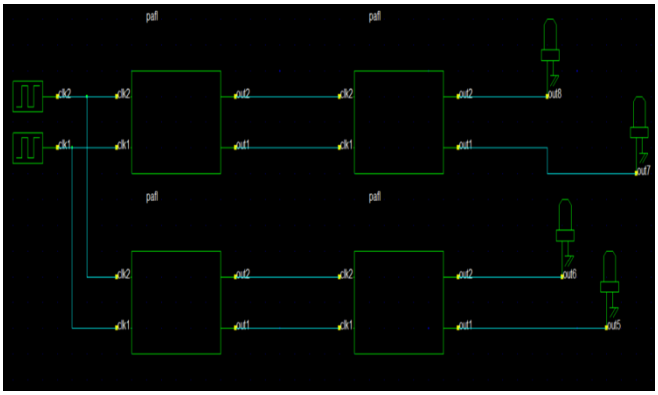
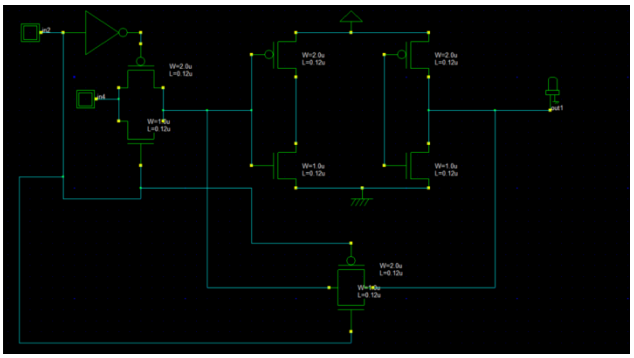
EXTENSION MODEL FOR T_FF:



Similarly we have modelled and proposed the similarly changed Dual-DFF to design a toggling model for each values of out2 mentioned in the circuit. The purpose of the in1 is provide stage by stage design control over the output data ensuring the correct sequence of the data is assured at each values of the input data given.

CIRCUIT 1:



Here we have seen the current Dual-D ff design with respect to 10 Transistor with 32 nanometer technology at each design frame. The above circuit aims to implement the D-FF with the two circuits presenting the don't care condition for the logic design.

CIRCUIT2:

The below circuit describes the control is modelled with the input1 as shown figure below. At each input values ie 0 or 1 would present a partial X values observed at out1 resulting don't care condition using pull up or pull down approach for the CMOS inverter. Since the PAFL circuit would provide the design implementing the design platform would estimate the output 0 at input 0 and clock 0 and X at clock 1. Similarly for input 1 the clock 1 would provide the outputs value as 1.

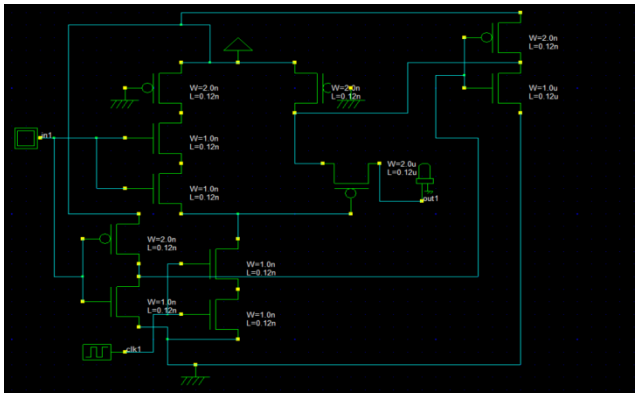


Figure : Representing the D-X flip flop using CMOS gates.

CONCLUSION

For various switching activities power dissipated by the clock and power dissipated by the rest of the flip-flop have

been estimated. It is clearly seen that power dissipated by the clock and power dissipation of the rest of the circuit is less in case of sleep mode in SCCER and DCCER flip-flops as in case of exisinting model. The proposed design model emhasizng a Dual D- FF with and without Don't care condition. This design has proven better results when compared with the design on the sleep mode SCCER flip-flop has better performance. In active mode this design act as T-FF rather than D-FF resulting better performance than DCCER flip-flop. The clock gating scheme is implemented without any clock overload. This SCCER flip-flops can be used in adiabatic clocking in digital systems as they have good power and delay characteristics.

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