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Low Power 4x4 Bit Multiplier Design Using Dadda Algorithm And Optimized Full Adder

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Abstract- This paper presents the model of 4-bit multiplier having low power and high speed using Algorithm named Dadda and the basic building block used is optimized Full adder having low power dissipation and minimum propagation delay. Full and half adder blocks have been designed using pass-transistor logic and CMOS process technology to reduce the power dissipation and propagation delay. We have also applied Dadda algorithm to reduce the propagation delay. Simulations are performed by using MICROWIND 3.5 tool using Verilog file on 65nm technology. At first, using DSCH 3.5 Tool the circuits are implemented, and generated the Verilog file.

Keywords— Dadda Algorithm, Hybrid Design, Optimized Full Adder, 4×4 Bit Multiplier

I. INTRODUCTION

Multiplication is basic function in arithmetic operations. Multiplication based operations such as multiply and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), filtering are widely used in signal processing applications. As, multiplication dominates the execution time of DSP systems, there is need to develop high speed multipliers. Building blocks used in multipliers are a full adder and a half adder. Different design implementations of a full adder and half adder circuits have been used to reduce power and delay in order to design an optimized multiplier circuit which includes pass transistor logic, CMOS process technology, split percentage data-driven logic and CMOS process technology. Besides this, different multiplication algorithms also have been used to achieve optimized power and delay product which includes Dadda, Wallace tree, and Vedic and Booth algorithms. The Recent multiplier used Reduced-sp-D3Lsum Adder and Dadda Algorithm technique. This design operates at high frequency and consumes less power as compared to previous designs, but still, power needs to be significantly reduced, so, it will help in the larger circuits where multiplier itself becomes the building block [8]. In proposed work, a multiplier has been designed in which Full adder and half adder has been used as its building block to reduce the power dissipation by using passtransistor logic and CMOS technology process. Dadda Algorithm has been used to reduce the propagation delay of the multiplier. The paper has been ordered according to this flow. Existing system regarding multiplier and full adder has been presented in Sect. II; proposed design is described in Sect. III; block diagramsandalgorithmimplementationarecovere dinSect. IV and V; results in Sect VI; while the conclusion is in Sect. VII. II. EXISTING SYSTEM Multiplier using Pass transistorlogictechniqueisonewhichusesareduced numberof transistors and offers small node capacitances which produces minimumdelayandincreasethespeedofthecircuit. Different techniques such as; merged delay

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transformation [1- 2], genetic algorithm [3-5], evolutionary algorithm [6], delay path Unequalization [7], carry-look-ahead logic [8], etc. have beenusedandimplementedtodesigndigitalcircuits havinglow power dissipation, minimum delay and to achieve maximum throughput in minimum response time. Techniques include pass-transistor logic CMOS process technology, adiabatic static CMOS logic, reversible logic, etc. Multipliers having reversible logic have reduced power dissipation. Multipliers' having adiabatic static CMOS logic produce minimum heat while transferring thecharges. III. PROPOSEDSYSTEM In the proposed system, a modified circuit of the 4*4 multiplier is proposed. This multiplier circuit is based on the optimized full adder which uses 12 transistors i.e., 12T. The design of full adder is hybrid i.e., the design consists of two techniques, pass-transistor logic, and CMOS process technology. Full adder and a half adder as the building block of the circuit have low propagation delay and low power delay product. The power and delay of this full adder are low as comparedtootherpreviousdesignedfulladders.Thi sultimately results in the formulation of multipliers having low propagation delay and minimum powerdissipation. A. DADDA TREEALGORITHM Different algorithms have been proposed to decrease the propagation delay during the addition of the partial products generated by AND Gate. One of the most efficient algorithmsis Dadda algorithm. The proposed 4*4 multiplier has a total of 16 partialproducts,so,theheightofthetreeisfourassho wnFig. 1. Dadda Algorithm has been applied for the purpose to reduce theheightofthetreefromfourtotwo.If wedonotapplyDadda algorithm, then we must have to wait for the previous stage to simulateit,because,thenextstageusesthecarryofth eprevious stage which will increase the propagation delay. For this simple technique, we have to use the ripple carry adder, it also consumes less power, but the delay is significantly high. To reduce the overall propagation delay of the multiplier Dadda algorithm has beenapplied. This is the best technique for reduction in the delay of the overallmultiplierdesignbecause,atthestart,itdoesn otdepend on the previous stage. Therefore, the first stage will be implemented without depending on any other stage. First, we have arranged our partial products to make a tree as shown in Fig.1.ThesepartialproductsaregeneratedbytheAN Dgate.

The height of this tree is 4 as the proposed design is the 4-bit multiplier.

B. STAGES OF DADDAALGORITHM

The objective is to reduce the height of the tree from four to two.Therefore, building blocks have been used in such a way to reduce the tree height from four to three after the completion of first Dadda stage and then from three to two after the completion of the second Dadda Stage. Furthermore, the two Dadda stages are used to reduce this tree. The first and second Daddastagesareshowninfig.2andFig.3,respe ctively.

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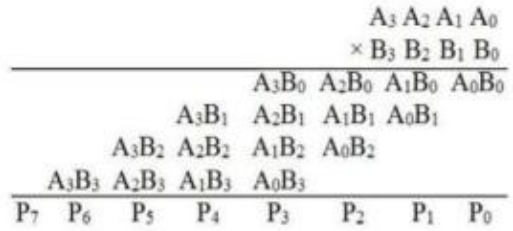

Figure 1: 4 × 4 Multiplications.

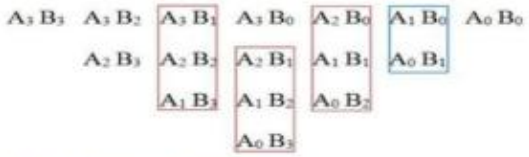

Figure 2: First Dadda Stage

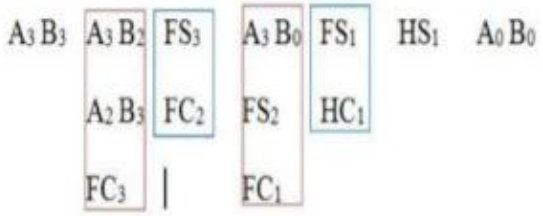

Figure 3: Second Dadda Stage

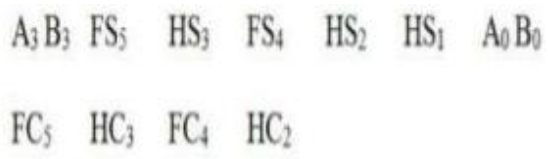

Figure 4: Last Dadda Stage

C. ALGORITHMIMPLEMENTATION

We apply the Dadda algorithm on this tree to reduce the height of the tree. At the first stage: tree has a height of 4 which we need to reduce by using full adders and half adders. Hence, we have applied a full adder on the 4th column to reduce its height also we have applied half adder on the 2nd column and two more full adders on the 3rd and 5th column to adjust the tree height to 3. Now these HA and FA are working in parallel and no one is dependent on the previous stage. Figure 3 and 4 shows the more tree reduction and in the final stage, we have used a ripple carry adder. The count of the half adder and full adder used in the Dadda stages are given by these formulas Halfadder=H-1 Fulladder=H2-4H+5

IV. BLOCKDIAGRAM

THE BLOCK DIAGRAM OF OUR PROPOSED MULTIPLIER IS SHOWN IN FIG.5.

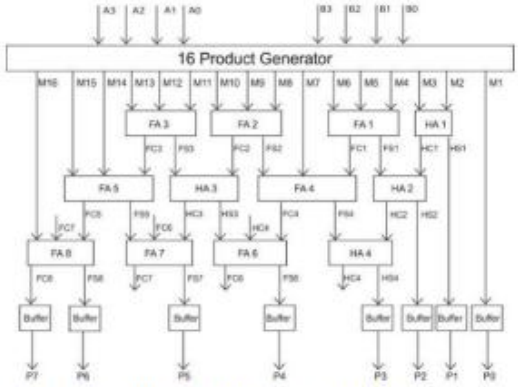

Figure 5: Block Diagram of the proposed Multiplier

The working stages of the proposed model are as follows: 1. In the first step,16partial products are generated using ANDgate. 2. In the second step, the height of the tree is reduced using Dadda stage using one-half adder (HA) and three full adders(FA). 3. In the third step, the reduction is done by two half adders and two fulladders. 4. At last stage of Dadda, we have used a ripple carry adder. 5. Finally, results are passed through the buffer to make the output voltages better(smooth).

V. BUILDINGBLOCKSOFPROPOSED MULTIPLIER THE BLOCKS THAT ARE USED IN THE PROPOSED DESIGN OF MULTIPLIER ARE AS UNDER:

A. ANDGATE

The proposed model has AND gate for the multiplication of 4*4 multiplier. Consequently, for the 4*4 multiplication, a

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total of 16 products are generated. Therefore, it has used 16 AND gates for multiplication. The schematic of the AND gate is shown in Fig. 6

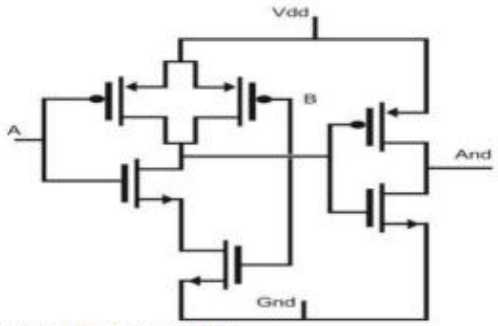

Figure 6: Two input AND gate.

B.FULLADDER A full adder is a major block in the multiplier. In proposed model Full adder has been modified in order to produce minimum propagation delay and less power dissipation of the circuit, so, that it can further be used to design multiplier having optimized parameters including Power, delay, and less layout area. Proposed modified XOR module in the Full adder is composed of four transistors. The schematic of the proposed XOR module is shown in Fig. 8. We have inverted one input i.e., B input because the B and B' will be used in the next two transistors. We have cascaded a PMOS with NMOS while applying the second input A to the gate terminal of both PMOS and NMOS and instead of connecting the source of the PMOS to Vdd we connected it to the first input B, similarly we have connected the source of the NMOS to the inverted first input i.e., B', which constitutes XOR module. The equation of the XOR moduleis: XOR=A'B +AB'

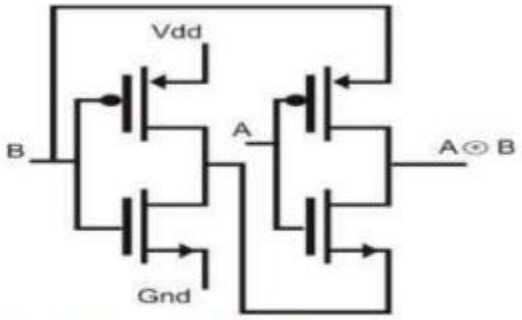

Figure 8: Proposed XOR Module

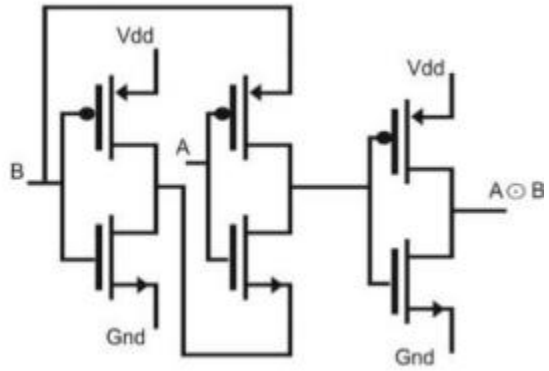

Figure 9: XNOR Module

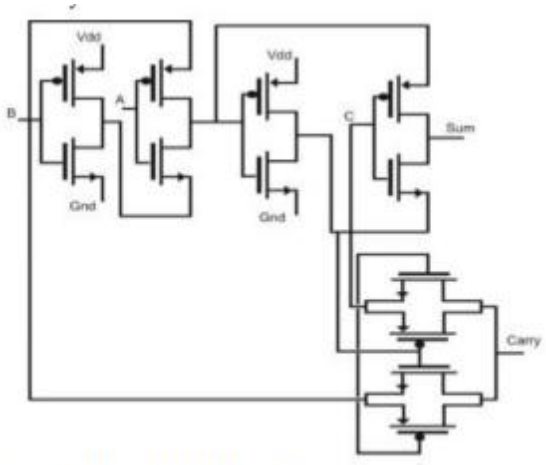

Figure 10: Proposed Full Adder

C.HALFADDER A half adder is another building block of the multiplier. We used total four half adders in the multiplier design. The schematic of the half adder is shown in Fig. 10.

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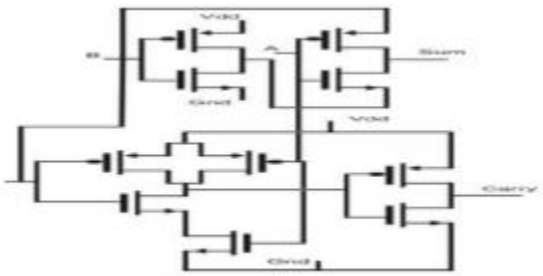

Figure 12: Half Adder

D.BUFFER The buffer is an amplifier having unity gain. The main function of the buffer is to provide drive capability to pass signals to the final stage. Voltage buffer is used to increase the available current for the circuits having low impedance while retaining the voltage level. On the other hand, current buffers keep the current same and drive the high impedance inputs at higher voltage levels.

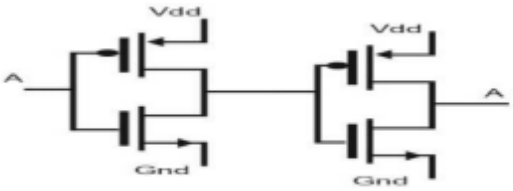

Figure 14: Buffer

V1 RESULTS

The proposed low power 4x4 multiplier using DADDA algorithm and optimized full adder , the circuits were designed using 65nm CMOS process in Micro wind, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance. The simulations were done using DSCH and micro wind with a power supply of 1V. Simulation result and digital schematic of some of the circuits are given below using DSCH 3.5 tool

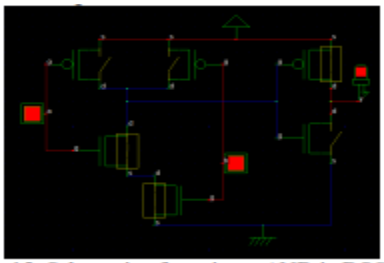

Figure 15: Schematic of two input AND in DSCH 3.5

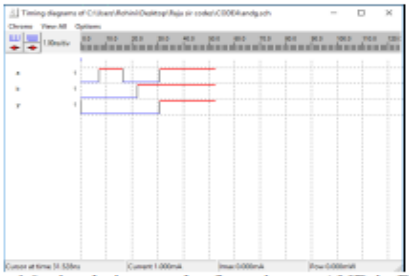

Figure 16: simulation result of two inputs AND in DSCH

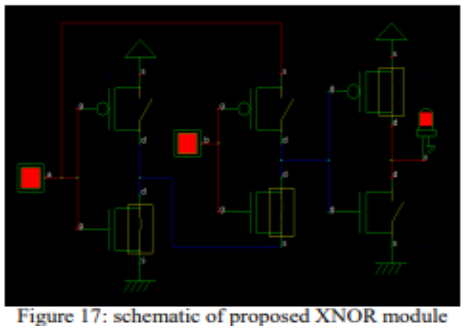

Figure 17: schematic of proposed XNOR module

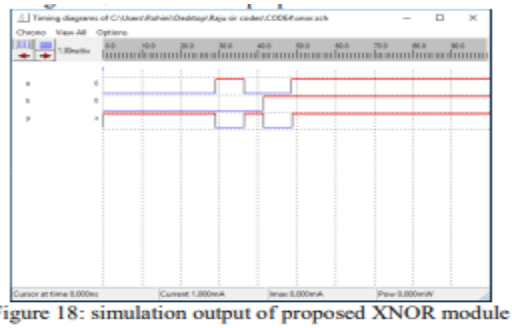

Figure 18: simulation output of proposed XNOR module

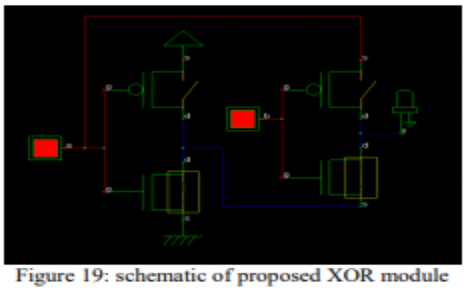

Figure 19: schematic of proposed XOR module

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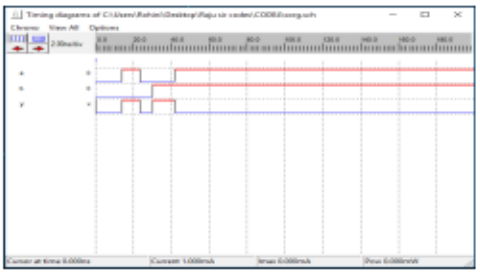
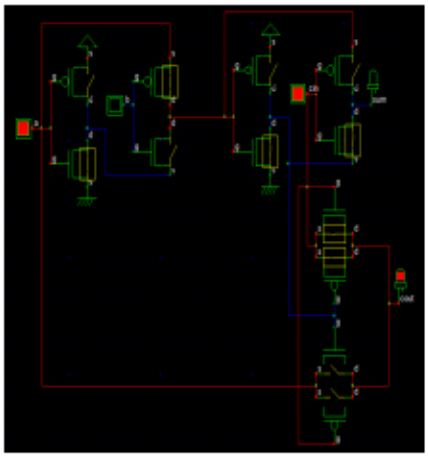


Figure 20: simulation result of proposed XOR module



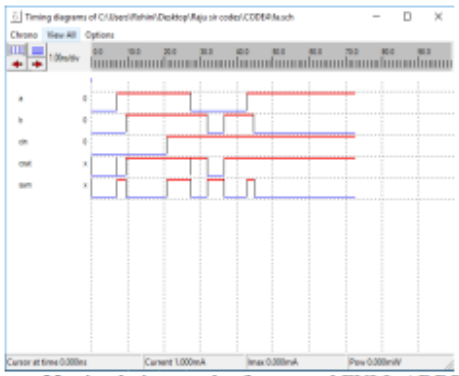


Figure 22: simulation result of proposed FULL ADDER

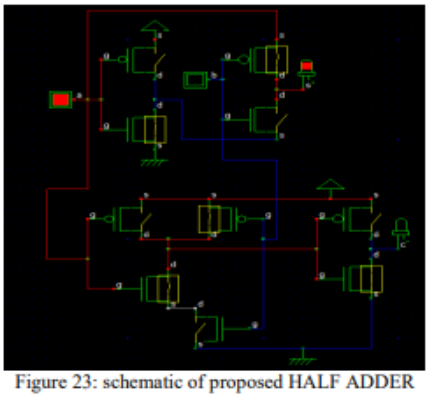


Figure 23: schematic of proposed HALF ADDER

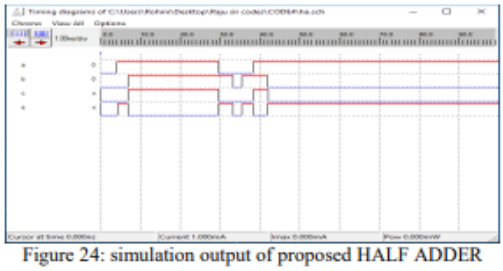


Figure 24: simulation output of proposed HALF ADDER

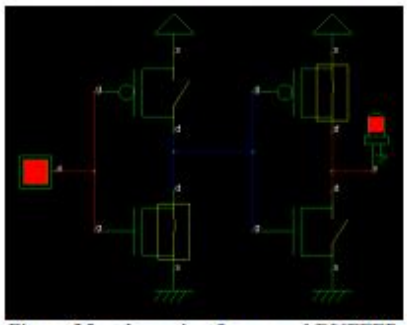


Figure 25: schematic of proposed BUFFER

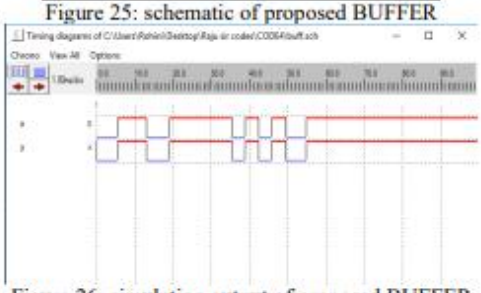


Figure 26: simulation output of proposed BUFFER

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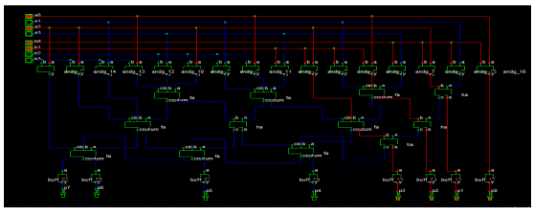

Figure 27: schematic of proposed 4x4 multiplier using DADD Algorithm and optimized full adder designed in DSCH

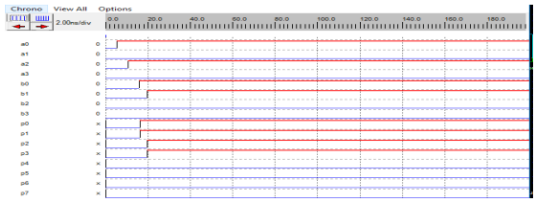

Figure 28: simulation output of proposed 4x4 multiplier

The Verilog files which are generated in DSCH are compiled in MICROWIND 3.5 and is implemented on CMOS 65 nm technology , from which we can calculate the power and number of transistors used to design the proposed circuit and can be compared with the existing design in terms of power and area and count of transistor.For the proposed 4*4 multiplier the inputs A3, A2, A1, A0, B3, B2, B1, and B0 are pulses varying from 0 to 1. The operating frequency of the proposed multiplier is 5 GHz. The comparison of the proposed multiplier with another multiplier is showninTable.4.

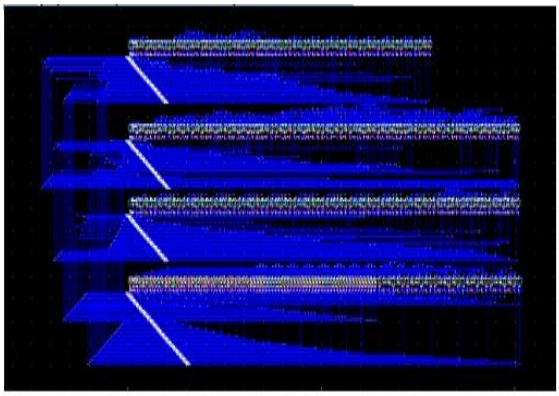

Figure 29: layout of proposed 4x4 multiplier on MICROWIND 3.5 using CMOS 65nm technology.

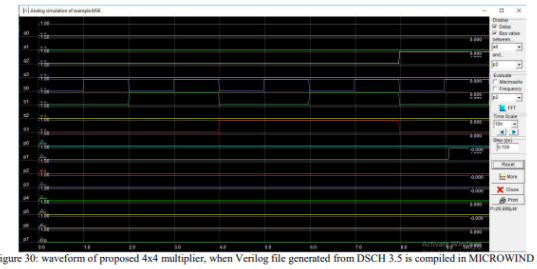

Figure 30: waveform of proposed 4x4 multiplier, when Verilog file generated from DSCH 3.5 is compiled in MICROWIND 3.5

IV COMPARISION TABLE

DESIGN	Area(μm^2)	power	frequency
Proposed	4470.6	26.986µW	5GHZ
Existing [6]	5430.2	59.6	3.81GHZ
Existing [8]	6325.8	79	3.39GHZ

VII CONCLUSION

The proposed model having high speed, low latency and minimum delay are being designed which has two modified circuits in it. One is hybrid full adder which has been designed by Pass transistor logic and CMOS process technology. Hybrid full adder has low propagation delay by which maximum throughput can be achieved in minimum response time. A highspeed 4*4 multiplier has been designed using the hybrid Full adder as its building block and Dadda Algorithm has been applied to achieve this. The proposed 4*4 multiplier operates at a frequency of 5GHz and has an average power of 26.986µW with a delay of 0.100nS.Multiplier having low latency, minimum power dissipation and less layout area have been designed by the proposed model.

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