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A NOVEL DESIGN OF HYBRIDIZED MULTIPLIER WITH HIGH SPEED AND LOW POWER

[1]P.RAJESH, [2]V. SADHVI, [3]P. SAI BHARGAVI, [4]P.AMRUTHACHANDANA, [5]Y. CHAITHANYA, [6]T. KAVYA, [7]S. KRISHNAVENI

[1]Assistant Professor, Department of ECE, Sree Venkateswara College of Engineering, Northrajupalem(VI), Kodavaluru(M), Nellore (DT), Andhra Pradesh, India.

[2,3,4,5,6,7]B.Tech Scholars, Department of ECE, Sree Venkateswara College of Engineering, Northrajupalem(VI), Kodavaluru(M), Nellore (DT), Andhra Pradesh, India.

ABSTRACT: The multiplier is the most basic unit of an arithmetic circuit which is predominantly used in digital processing units and several integrated circuits. The efficiency of a processing unit is measured by its speed and power consumption. The key problem VLSI circuits are high power consumption, larger area utilization and delay which affect the speed of computation and also result in power dissipation. For solving the issues, a novel design of Hybridized Multiplier with high Speed and Low Power is presented in this paper. In proposed system, high speed multiplier, modified booth multiplier (MBM) and Wallace tree multiplier are hybridized with carry look ahead adder (CLA) and formed a hybridized multiplier which delivers high speed computation with low power consumption. MBM is proposed to reduce the partial products whereas Wallace tree multiplier is accompanied for fast addition and CLA is used for final accumulation. This hybrid multiplier produces better results in terms of speed and power than the conventional designs.

KEYWORDS: Modified Booth Multiplier, Wallace tree multiplier, Hybridized Multiplier, carry look ahead adder.

I. INTRODUCTION

The essential need of VLSI circuits is high speed computation and low power consumption. Achieving the optimized result is highly challengeable since it is difficult to select and optimize Multipliers and adders which are responsible for computation. Multipliers and adders play an important role in VLSI for getting desired results. Multipliers are predominantly used in microprocessors and digital signal

Multiplication is a series repeated additions. Multiplicand is the number to be added, Multiplier is the number of times that it is added and product is the result. The modus operandi for multiplication in digital systems is repeated additions of partial products and the conventional multipliers require a large number of adders for partial product addition for higher order multiplication. The most basic multiplier is the array multiplier.

Several multiplier circuits have been designed over the years to reduce the number of partial products and also to improve speed, namely the Booth, the Wallace tree (WT), the Baugh-Wooley multipliers, etc [2]. These multipliers have been implemented in the conventional complementary metal oxide semiconductor (CMOS). Conventional logic designs like the static CMOS and the pass transistor logic (PTL) are vital in designing full adders in multipliers. The PTL offers advantage in terms of the number of transistors used within the adders. The C. S. Wallace proposed a technique for the partial product reduction tree (PPRT) using the full adder all the partial product can be added in parallel and Wallace tree is continuestill the final two rows of sum and carry [3]. The Wallace treestructure for the addition of the

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six partial products. Finally, an array of sum and carry is added to obtain the final product. All methods of multipliersmake use of the concept of Wallace reduction tree.
The multiplication of signed number is performed by using the Booth's multiplication algorithm. The Booth's multiplier makes use of the 2's complement number system to represent both the positive and negative operands. The Booth's multiplier replaces continuous 1's with 0's and thus the addition operation reduces and the speed of multiplication operation increases.

A binary multiplier is an electronic circuit utilized as a part of advanced gadgets, for example, a PC, to duplicate two binary numbers. It is fabricated utilizing binary adders. An assortment of PC number juggling strategies can be utilized to execute an advanced multiplier. Most systems include registering an arrangement of partial products, and afterward summing the partial products together. This procedure is like the technique educated to elementary school kids for leading long multiplication on base-10 whole numbers, however has been adjusted here for application to a base-2 (binary) numeral framework [4]

An ordinary binary (NB) multiplication by advanced circuits incorporates three stages. In the first step, partial products are created; in the second step, every partial product are included by a partial product diminishment tree until the point when two partial product lines remain. In the third step, the two partial product lines are included by a quick carry spread snake. Two strategies have been utilized to play out the second step for the partial product decrease. A first strategy utilizes four- two compressors, while a moment technique utilizes redundant binary (RB) numbers. The two strategies permit the partial product lessening tree to be diminished at a rate of 2:1. The redundant binary number portrayal has been acquainted by Avizienis with perform marked digit math; the RB number has the capacity to be spoken to in various ways. Quick multipliers can be outlined utilizing redundant binary addition trees.

A new architecture has been proposed by the hybridization of modified booth multiplier, Wallace tree multiplier and carry Look-ahead adder [5]. This hybrid multiplier is mainly focused for reducing the partial products and to trigger the speed of the computation. MBM generates n/2 partial products for „n‟ inputs so the area is directly reduced and increases the speed of the computation. Wallace tree is designed to carry save adders (CSA) which is used for fast addition since 3:2 compressors are used. It is responsible for fast addition. The results of CSA are finally getting computed by Carry Look-ahead adder which is mainly proposed for final accumulation.

II. LITERATURE SURVEY

N. Prajwal, S. K. Amaresha, Siva S Yellampalli, et. al. [6] introduces a new modified compressor based multiplier architecture. This structure uses the 3-2, 4-2, 5-2 and 7-2 compressors architecture which has less area compare to normal adders. The comparison was made on synthesis results of all other adder, comparison shows that the new introduced adders consume less area and power. In addition to that it uses Vedic multiplier and unsigned Baugh-wooley Wallace tree multiplier to increase the performance of multiplier with less area and power. The ASIC Implementation can be done using Cadence 45nm CMOS technology. Further optimization can be

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done using other physical design optimization algorithm.

Jakia Sultana, Sajib Kumar Mitra, Ahsan Raja Chowdhury, et. al. [7] presents a design methodology for the realization of Booth's multiplier in reversible mode. Booth's multiplier is considered as one of the fastest multipliers in literature and we have shown an efficient design methodology in reversible paradigm. The proposed architecture is capable of performing both signed and unsigned multiplication of two operands without having any feedbacks, whereas existing multipliers in reversible mode consider loop which is strictly prohibited in reversible logic design. Theoretical underpinnings, established for the proposed design, show that the proposed circuit is very efficient from reversible circuit design point of view.

M Mohamed Asan Basiri, Samaresh Chandra Nayak, Noor Mahammad Sk, et. al. [8] proposes a novel fixed point multiplier architecture with data level parallelism. Here, author proposed a Wallace tree multiplier to perform more number of multiplications in parallel with fewer extra carry save stages than conventional multiplier. The proposed n-bit Wallace structure is used to perform four (n/2)×(n/2)-bit multiplications, two n×(n/2)-bit multiplications and one n × n-bit multiplication in parallel. The proposed system is having slightly higher depth than conventional multiplier due to 2 extra carry save stages to incorporate multiple multiplications in parallel, which is not possible in conventional Wallace tree multiplier.

Sushma R. Huddar, Sudhir Rao Rupanagudi, M. Kalpana, Surabhi Mohan, et. al. [9] introduce a novel architecture to perform high speed multiplication using ancient Vedic maths techniques. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been explored. Upon comparison, the compressor based multiplier introduced in this paper, is almost two times faster than the popular methods of multiplication. With regards to area, a 1% reduction is seen. The design and experiments were carried out on a Xilinx Spartan 3e series of FPGA and the timing and area of the design, on the same have been calculated. R. Mahalakshmi, T. Sasilatha, et. al. [10] presents A power efficient carry save adder and modified carry save adder using CMOS technology. Adders form an almost obligatory component of every contemporary integrated circuit. The primary requirement of the adder is that it is fast and efficient in terms of power consumption and chip area. In this paper we design a CMOS Logic based Carry Save adder and Modified carry save adder and to deliver with 250 nm, 65nm technology with low power by replacing the architecture for minimal power utilization.

III. DESIGN OF HYBRIDIZED MULTIPLIER

Hybrid multiplier comprises of a Modified Booth encoder block cascaded to the Wallace Tree and finally summed by the Carry Look Ahead Adder. As shown in the figure, recoding of the bits is done at the first stage in parallel at all the bit positions thereby minimizing latency. By using the carry save adders the speed is further improved as the carries are saved instead of propagated. The partial sum and carry are then given to the CLA to obtain the multiplication result. This hybrid multiplier

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is mainly focused for reducing the partial products and to trigger the speed of the computation. MBM generates n/2 partial products for „n" inputs so thearea is directly reduced and increases the speed of the computation. Wallace tree is designed to carry save adders (CSA) which is used for fast addition since 3:2 compressors are used. It is responsible for fast addition. When the input is signed, the 2's complement of that number will be taken then it will be processed for generating outputs. After the generation of partials the output products will be given to the Wallace tree multiplier for fast addition. CSA performs the addition faster than other adders and delivers the output to the CLA. It is used for final accumulation and yields the final result.

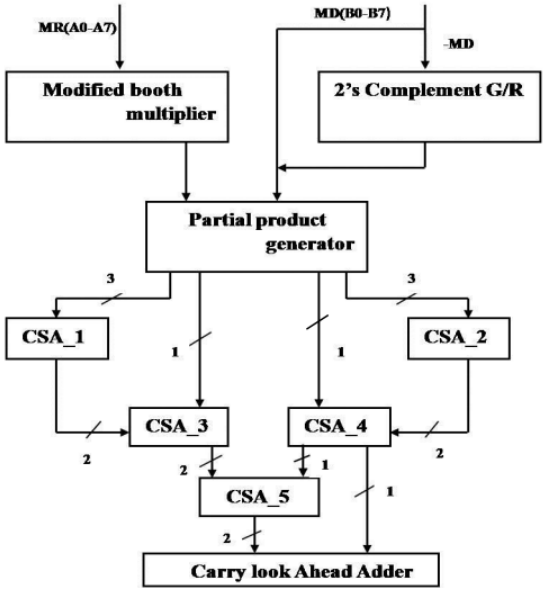

Fig. 1: HYBRID MULTIPLIER

The multiplication of signed number is performed by using the Booth's multiplication algorithm. The Booth's multiplier makes use of the 2's complement number system to represent both the positive and negative operands. The Booth's multiplier replaces continuous 1's with 0's and thus the addition operation reduces and the speed of multiplication operation increases. The single bit recoding method is very slow and worst case produces n-number of partial products. The fast multiplier is designed by using the Modified Booth's Encoder (MBE) multiplier also called bit pair recoding. In this technique the number of partial product is half the partial products compared to the Booth recoding technique.

The Wallace multiplier is a parallel multiplier that is very efficient. The first step in constructing a partial product array in a Wallace multiplier is to create a partial product array (of N^2 bits). Groups of three adjacent rows are collected in the second stage. By employing full adders and half adders, each set of three rows is decreased. When there are three bits in a column, full adders are used, and half adders are used when there are only two bits. Each bit in a column is transmitted unprocessed to the next stage in the same column. In each subsequent stage, the reduction method is repeated until only two rows remain. In the last stage, a carry propagating adder is used to add the remaining two rows. Finally, an array of sum and carry is added to obtain the final product. When an M-bit multiplier is multiplied by an N-bit multiplicand, the multiplier creates M*N product terms. The full adder, which adds several operands, is used to add the product terms formed. The ultimate product of the M*N multiplier is (M+N) bits size, which is the outcome of the multi operand addition (MOA).

IV. IMPLEMENTATION ANALYSIS

The last step in the design process involves configuring the designed circuit in an actual FPGA device. To show how this is done, itis assumed that the user has access to the

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Altera DE2 Development and Education board connected to a computer that has Quartus II software installed. A reader who does not have access to the DE2 board will still find the tutorial useful to learn how the FPGA programming and configuration task is performed.

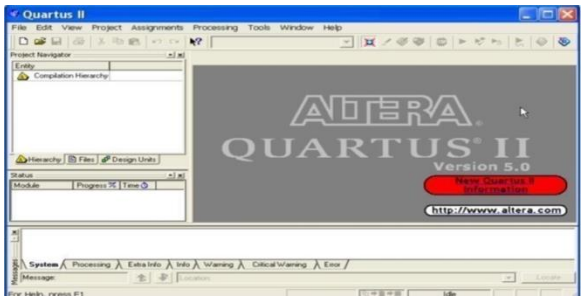

Fig. 2: THE MAIN QUARTUS II DISPLAY

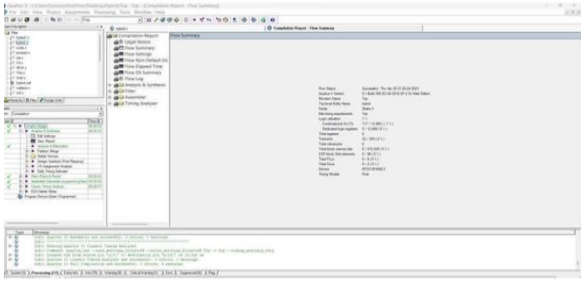

Fig. 3: COMPILATION REPORT OF 8-BIT HYBRID MULTIPLIER

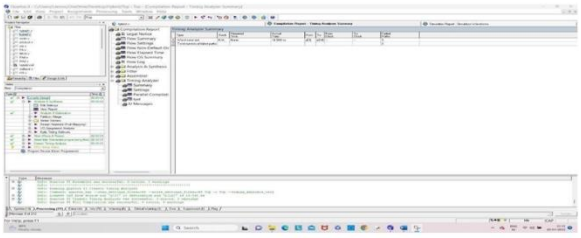

Fig. 4: TIMING OF 8-BITHYBRID MULTIPLIER

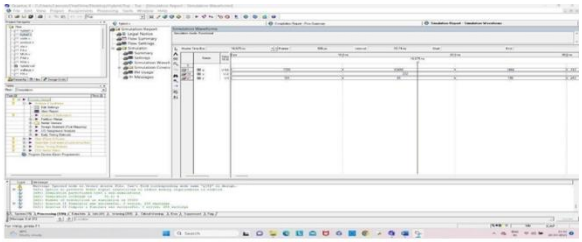

Fig. 5: SIMULATION REPORT OF 8-BIT HYBRID MULTIPLIER

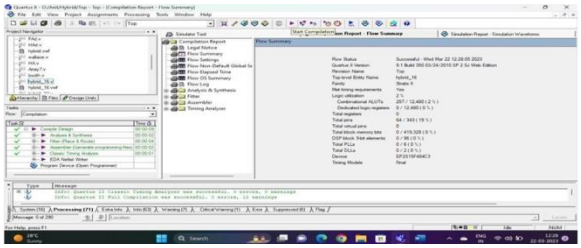

Fig. 6: COMPILATION REPORT OF 16-BIT HYBRID MULTIPLIER

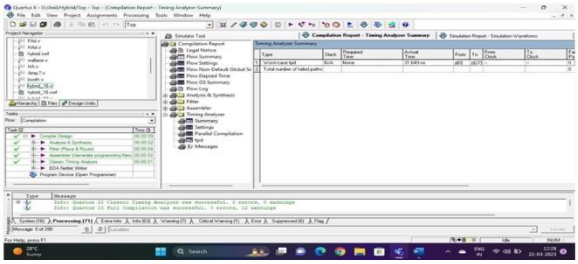

Fig. 7: TIMING OF 16-BITHYBRID MULTIPLIER

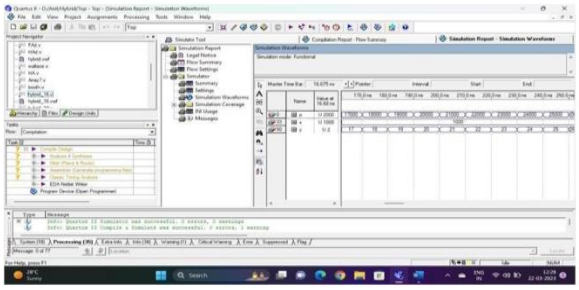

Fig. 8: SIMULATION REPORT OF 16-BIT HYBRID MULTIPLIER

Table 1: PERFORMANCE ANALYSIS

Architecture	Power (μw)	Delay (ns)
Array-7 bit	18540	22.113
Wallace-8 bit	490.7	16.917
Booth-8 bit	2666	16.65
Hybrid-8 bit	301	13.52

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Hybrid-16 bit	306	31.649
Hybrid-32 bit	316	36.29
Hybrid-64 bit	356	44.91

Therefore, the Hybrid multiplier is efficient in terms of delay and power than other conventional multipliers.

V. CONCLUSION

In this paper, a novel design of Hybridized Multiplier with high Speed and Low Power is described. The Hybrid Architecture is the combination of high-speed multipliers and adders. In proposed system, high speed multiplier, modified booth multiplier (MBM) and Wallace tree multiplier are hybridized with carry look ahead adder (CLA) and formed a hybridized multiplier. The design can be used for meeting the challenges in all signal processing applications by its faster operations. The speed of the computation is increased since the partial products are reduced. To reduce the delay and area of the multiplier, the final product of multiplier is calculated by each two consecutive multiplicand bits of partial products added simultaneously using different-sized hybrid adders. Therefore, the Hybrid multiplier is efficient in terms of delay and power than other conventional multipliers.

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