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Quaternary Logic Circuit designs using Graphene Nanoribbon Field Effect Transistors

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Abstract: The implementations of quaternary circuit schematics are presented in this paper. The quaternary logic is a better choice over the conventional logics because it offers high operating speed, reduced chip area and reduced on-chip interconnects. A new method is presented to design quaternary schematics using graphene nanoribbon field effect transistors (GNRFETs). The dimer line of graphene nanoribbon (GN) is used to control the threshold voltage of GNRFETs. Four quaternary logic inverter circuits such as standard quaternary inverter (SQI), intermediate quaternary inverter (IQI), positive quaternary inverter (PQI) and negative quaternary inverter (NQI) along with the NAND and NOR circuits are proposed. Furthermore, the quaternary half adder circuit is designed that helps to develop complex designs. The HSPICE simulator is utilized for simulating the proposed designs to obtain the performances such as delay, power and power delay product (PDP). The obtained circuit performances are compared with carbon nanotube FETs (CNTFETs) based circuits. The comparison results show that the proposed GNRFET circuits achieved 53.51% of overall performance improvement over the CNTFET circuits.

Keywords: GNRFET, quaternary, quaternary half adder and HSPICE.

1. Introduction

Generally, the digital computations are associated with the two valued logic (TVL), i.e., logic 0 and logic 1 which are equivalent to voltages 0 and V_{DD}, respectively. In recent days, the multiple valued logic (MVL) captivated the researchers due to its several advantages than the TVL such as reduced interconnect complexity, high bandwidth, large transmission of data, reduced chip area, faster operations and more data storage [1-4]. Thus, the simplicity and energy efficiency in digital system can be achieved for MVLs. The MVL consent more than two logic states and, based on number of logics, it is categorized into ternary (base = 3) or quaternary (base = 4) or quinary (base = 5) logics [1, 4]. The quaternary logic has drawn more attention from the research community over the ternary and quinary logics. In quaternary logics, the logic states 0, 1, 2, and 3 represent the voltages 0, $0.3V_{DD}$, $0.6V_{DD}$, and V_{DD}, respectively [2]. For comparison of TVL and MVL, a multiplier circuit is compared in [5]. The MVL based multiplier shows the 50% performance enhancement as for power consumption and chip area over the TVL multiplier. The detailed study on the designs of MVL complementary metal- oxide-semiconductor (CMOS) is presented in [6-8].

The MVL circuits design mainly needs the multiple threshold devices (MTDs). The MTDs in MOS technology can be developed utilizing the bulk bias technique. However, biasing bulk regions of MOSFETs is a hard task. Additionally, short-channel problems, drain induced barrier lowering, shrinking problems, large power consumption, and other signal integrity effects can be occurred with the MOSFETs [4]. Thus, various novel materials and techniques like single electron transistors [9], quantum dot transistors [10], reversible logic transistors [11], and graphene based transistors [1-4] are being explored to avoid these effects. Out of them, graphene based transistors attracted the researchers for developing the MVL circuits due to its large mobility, ballistic transport, and large mean free path [1-4].

Graphene based transistors are categorized as CNTFET and GNRFET. Now-a-days, the CNTFET and GNRFET become trendy research topics in the field of nanoelectronics. However, the CNTFET experiences various challenges such as gate alignment problem and incompatible with planner technology [4]. Alternatively, due to the planner structure, the GNRFET is more compatible compared to the CNTFET. Moreover, the GN has better properties over carbon nanotube (CN) [12]. The GNs also provides the higher performance than CNs because of its smooth edges and reduced defects [13]. Additionally, the current driving ability is improved by introducing more GN channels in the FET. Thus, utilizing GNRFET for MVL circuits provides high performance and throughput over the CNTFETs.

In GNRFETs, the threshold voltage (V_{GN}) is operated by the width of GN. Thus, MTDs can be developed by employing various GN widths [14]. Utilizing multiple threshold GNRFETs, the MVL schematics are designed in [1]. In their work, basic logic and adder circuits are developed. The performance of these designs is compared with CNTFET based designs. The GNRFET designs reduced the delay and area up to 41.3% and 64% compared CNTFET circuits. The designs of GNRFET based half adder and multiplexer in ternary logics are discussed in [4]. The ternary to binary decoder is implemented to develop adder that degrades the complexity of the circuit. It is observed that the GNRFET based adder and multiplexer shows high performance in terms of power dissipation, propagation delay and PDP over the conventional MOS and CN technologies. The various GNRFET based logic and arithmetic schematics are developed with supply voltage 0.5V in [14]. The performance of these designs is noticed in terms of PDP for various channel and oxide thickness. Additionally, PDP of the proposed designs is compared to CNTFETs. The GNRFET based schematics show improved PDP over the conventional CNTFETs. In [15], two design techniques were presented to develop the ternary half adder. The first design technique utilizes 52 CNTFETs and 8 resistors and second design technique uses 58 CNTFETs. It is noticed that the design techniques have reduced the delay over conventional design techniques. The resistive and transistor based quaternary inverters using GNRFETs are presented in [16]. From the analysis, it is observed that the transistor based inverter provides a 61.1% reduction in PDP compared to the resistive based inverter.

Due to the advantages of MVL and GNRFETs, the detailed design of GNRFET based quaternary basic logic and arithmetic designs are proposed in this work. The numerical equations to relate the GN dimer value, bandgap, width, and V_{GN} are discussed. The bandgap and V_{GN} are calculated utilizing the

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numerical equations and validated with the quantumwise ATK for different GN dimer line values. The voltage and current (V-I) curves are also presented. Then the quaternary logic inverters, universal gates, and half adder circuit are presented. The voltage transfer characteristics (VTC) of inverters are also discussed. The performance of the proposed quaternary GNRFET schematics is compared to traditional CNTFET circuits.

The major highlights of this work are fivefold:

- The GNRFET based quaternary basic gates and arithmetic circuits are developed.
- The quaternary adder circuit is developed that used to implement the complex circuits.
- Numerical equations are discussed to calculate the GN dimer line, bandgap, width, and V_{GN} values.
- The proposed model is verified with the quantumwise ATK simulator.
- The performance of the GNRFET circuits is compared to the traditional CNTFETs.

2. GNRFET as quaternary logic devices

Graphene is a carbon allotrope belongs to a fourteenth group material and has four electrons in the valence shell. Because of four electrons in outermost band, the atoms of carbon create covalent bonds to the adjacent atoms and exhibits conductive nature. Naturally, the carbon is found to be many various conductive forms. The several wonderful properties are observed when the atoms of carbon are organized in honey comb lattice structure. The CN and graphene are the most popular carbon allotropes broadly explored as the alternative to MOSFET channels [4]. Graphene is layer of carbon atoms have a zero bandgap and behaves as excellent conductor. To open the bandgap and form semiconductor, the graphene must be transformed into thin strips (GNs) with width lower than 10nm [17]. The GNs are classified as zigzag GN and armchair GN. The zigzag based GNs always act conductive nature, while armchair based GNs shows either conductive or semi-conductive characteristics based on the dimer line value (m).

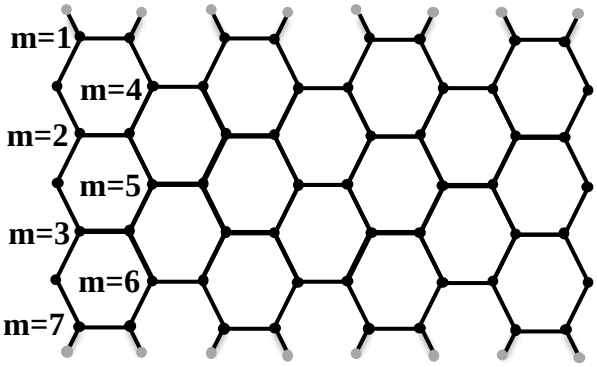

Fig. 1. Structure of armchair GN.

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The physical structure of armchair based GN with dimer line value (m) is shown in Fig. 1. For m = 3q or m = 3q + 1, the armchair GN acts as a semiconductor. Whereas, for m = 3q + 2, it acts as conductor [1]. The bandgap of GN (E_{gp}) given in equation (1) is utilized to confirm the semi-conductive and conductive characteristics of armchair GNs.

$$E_{gp} = \frac{2|\lambda| h V_{fr} \pi}{W_{GN}} \tag{1}$$

$$W_{GN} = \frac{\sqrt{3}(1+m)a_0}{2} \tag{2}$$

where W_{GN} is the width of GN, h is the Planck's constant, V_{fr} is the Fermi velocity, a_0 is the C-C bond distance, and λ is 0.066 for 3q+2, 0.4 for 3q+1, and 0.27 for 3q, respectively. Moreover, the E_{gp} is calculated of different m values of GNs and placed in Fig. 2. The E_{gp} values are also validated with the quantumwise ATK simulations and shown in Fig. 2. It is observed that the E_{gp} values are inversely proportional to m. It is also observed that the E_{gp} is small for m = 3q+2 and it acts as a conductor. Thus, in this study, the armchair GNs when m = 3q or 3q+1 can be utilized as channel in GNRFETs.

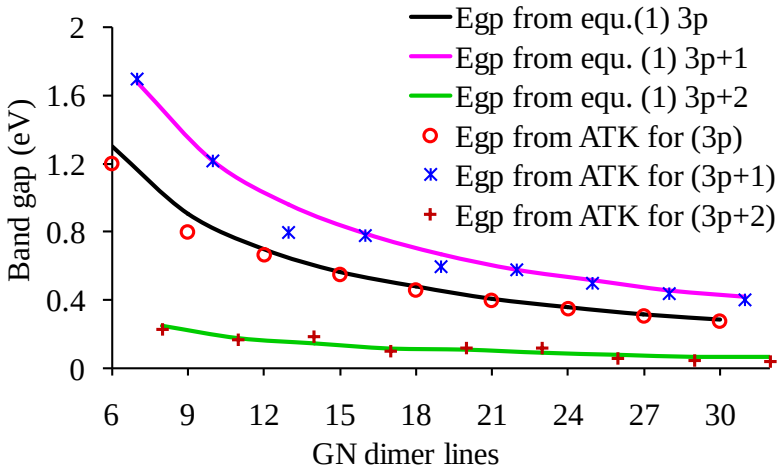

Fig. 2. GN bandgaps for various dimer line values.

Fig. 3 shows the physical structure of GNRFET. In GNRFETs, the heavily doped GN sheets are placed under the source and drain terminals whereas undoped layer is arranged beneath the gate. In GNRFETs, the source and drain regions can be doped either with donors or acceptors. Doping source and drain regions with donors is called as NGNRFET, whereas doping source and drain with acceptors is called as PGNRFET. The NGNRFET model is discussed detail in [17]. The threshold voltage of GNRFET is stated as

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$$V_{GN} = \frac{E_{gp}}{3e} \tag{3}$$

where is e is the charge of an electron. The GN width for seven dimer value is calculated as 0.98nm from equation (2) and threshold voltage is 0.56V from the equation (3). The calculated threshold voltages for different GN dimer line values are given in Table I. The threshold values found inversely proportional to dimer line values. Furthermore, the calculated values of threshold voltages are validated with the simulations for both NGNRFET and PGNRFET. The I-V characteristics of NGNRFET are shown in Fig. 4 for various GN dimer lines using SPICE simulator. The high drain current is obtained for high dimer value. Because of different threshold values and I-V curves possibilities, the GNRFET is suitable for quaternary logic designs.

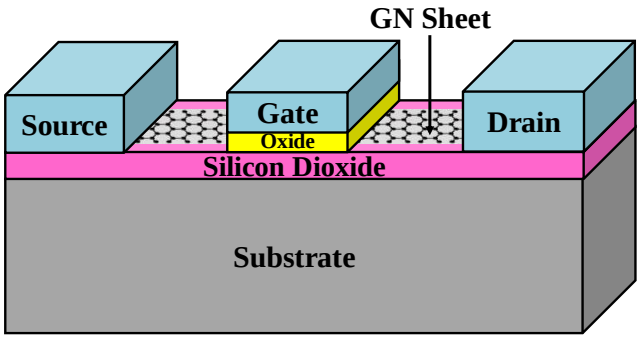

Fig. 3. Structure of GNRFET.

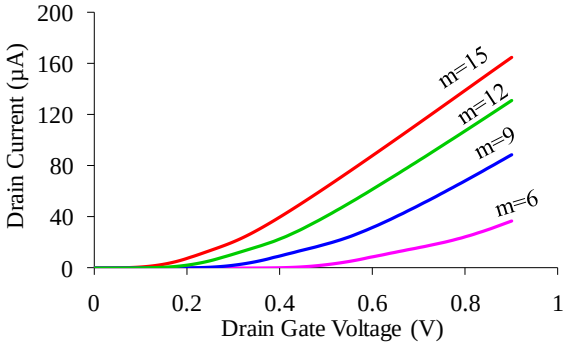

Fig. 4. V_{GS} versus I_{DS} curves when V_{DS}=0.9V

Table I: Threshold voltages of GNRFET for various GN dimer lines

GN Dimer line		Threshold Voltage (V)			
		Calculated Values		Simulated Values	
		n-channel GNRFET	p-channel GNRFET	n-channel GNRFET	p-channel GNRFET
3q	6	0.43	-0.43	0.42	-0.42
	9	0.30	-0.30	0.28	-0.28
	12	0.23	-0.23	0.22	-0.22
	15	0.19	-0.19	0.15	-0.15
	18	0.16	-0.16	0.11	-0.11
3q+1	7	0.56	-0.56	0.62	-0.62
	10	0.40	-0.40	0.40	-0.40
	13	0.32	-0.32	0.32	-0.32
	16	0.26	-0.26	0.24	-0.24
	19	0.22	-0.22	0.21	-0.21

$$SQI = 3 - a$$
$$IQI = \begin{cases} 3 if\ a = 0 or 1 \\ 0 if\ a = 2 or 3 \end{cases}$$
$$NQI = \begin{cases} 3 if\ a = 0 \\ 0 if\ a \neq 0 \end{cases} \quad (4)$$
$$PQI = \begin{cases} 3 if\ a \neq 3 \\ 0 if\ a = 3 \end{cases}$$

3. Survey of quaternary logic circuits

The functions of quaternary logic are realized by introducing the fourth value in the ternary logic. The operations of various quaternary logic circuits such as inverters, basic and universal gates, and half adder are specified as follows

3. 1 Quaternary logic inverters

In quaternary, four types of inverters such as SQI, IQI, NQI, and PQI are used [2]. The logic symbols and truth table of these inverters are shown in Fig. 5 and Table II, respectively. The quaternary inverter is operated with one input and four outputs and defined in equation (4).

3. 2 Quaternary logic gates

The operations of quaternary gates such as AND, OR, NOR and NAND are justified by analyzing the inputs *a* and *b*, respectively. The relation between inputs and outputs of these logic gates is defined in equation (5) and the truth tables are given in Table III. Fig. 6 shows various representations of logic gates.

$$AND = \text{minimum}(a\ and\ b)$$
$$NAND = \overline{\text{minimum}(a\ and\ b)}$$
$$OR = \text{maximum}(a\ and\ b) \quad (5)$$
$$NOR = \overline{\text{maximum}(a\ and\ b)}$$

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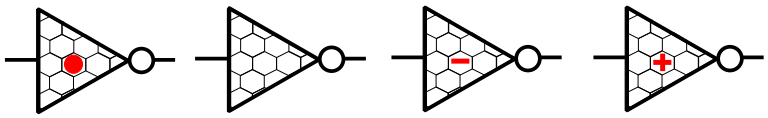
Table II: Truth table of SQI, IQI, NQI and PQI

A	Output			
	SQI	IQI	NQI	PQI
0	3	3	3	3
1	2	3	0	3
2	1	0	0	3
3	0	0	0	0

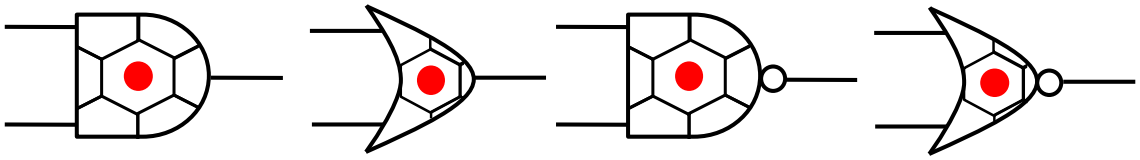


(a) (b) (c) (d)

Fig. 5. Quaternary inverters (a) SQI (b) IQI (c) NQI and (d) PQI.

Table III: Truth table of logic gates

Inputs		Outputs			
a	b	AND	NAND	OR	NOR
0	0	0	3	0	3
0	1	0	3	1	2
0	2	0	3	2	1
0	3	0	3	3	0
1	0	0	3	1	2
1	1	1	2	1	2
1	2	1	2	2	1
1	3	1	2	3	0
2	0	0	3	2	1
2	1	1	2	2	1
2	2	2	1	2	1
2	3	2	1	3	0
3	0	0	3	3	0
3	1	1	2	3	0
3	2	2	1	3	0
3	3	3	0	3	0



(a) (b) (c) (d)

Fig. 6. Quaternary logic gates (a) AND (b) OR (c) NAND and (d) NOR.

3. 3 Quaternary half adder

The quaternary logic circuits discussed above are utilized to develop the complex designs such as adders, multipliers, and memories. This work presents the design of quaternary GNRFET based half adder. The truth table and mathematical expressions to generate the sum and carry functions of quaternary adder is placed in Table IV and (6). The sum value of quaternary adder is high for the inputs (*a*, *b*) are (0, 3), (1, 2), (2, 1) and (3, 0). Hence, the quaternary based decoder is required to produce the unary operators for the utilized inputs. The quaternary decoder outputs for the input variable *a* are given in Table V and the circuit schematic is placed in Fig. 7.

Table IV: Half adder truth table

Inputs		Outputs	
a	b	sum	carry
0	0	0	0
0	1	1	0

$$\text{Sum}=3\cdot(a_0b_3+a_1b_2+a_2b_1+a_3b_0)+2\cdot(a_0b_2+a_1b_1+a_2b_0+a_3b_3)+1\cdot(a_0b_1+a_1b_0+a_2b_3+a_3b_2) \quad (6)$$

$$\text{Carry}=1\cdot(a_1b_3+a_2b_2+a_2b_3+a_3b_1+a_3b_2+a_3b_3)$$

Table V: Decoder Input and output values

a	a_0	a_1	a_2	a_3	a_i	$\overline{a_1}$	$\overline{a_2}$
0	0	0	0	3	3	0	3
1	0	3	0	3	3	3	3
2	0	0	3	3	0	0	0
3	0	0	0	0	0	0	3

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0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

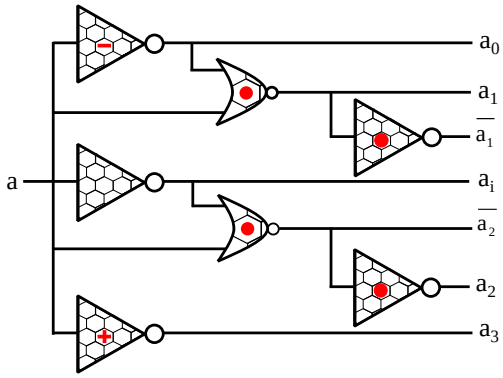

Fig. 7. Proposed quaternary GNRFET based decoder circuit.

4. GNRFET based quaternary logic design and operation

The GNRFET based quaternary inverters and universal gates are presented. Then the quaternary GNRFET based half adder design also presented. Furthermore, the performances such as delay, power and PDP for proposed quaternary designs are examined to CNTFET circuits.

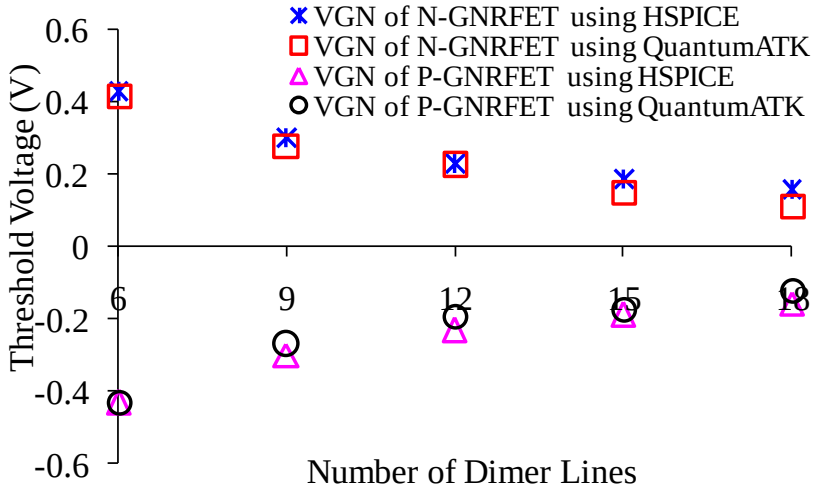

Fig. 8. Threshold Voltage values (V_{GN}) of GNRFETs.

The GNRFET SPICE model discussed in [17] is used for the implementing the GNRFET quaternary circuits. Using this model, the accurate and circuit compatible GNRFET can be developed. Moreover, the complete trans capacitance electronic circuit is involved in this model for high performance. For validation, the model is developed in QuantumATK to analyze the threshold voltages for various GN dimer lines and compared with the HSPICE threshold voltages. The obtained threshold voltages are shown in Fig. 8. The QuantumATK and HSPICE threshold voltages look similar.

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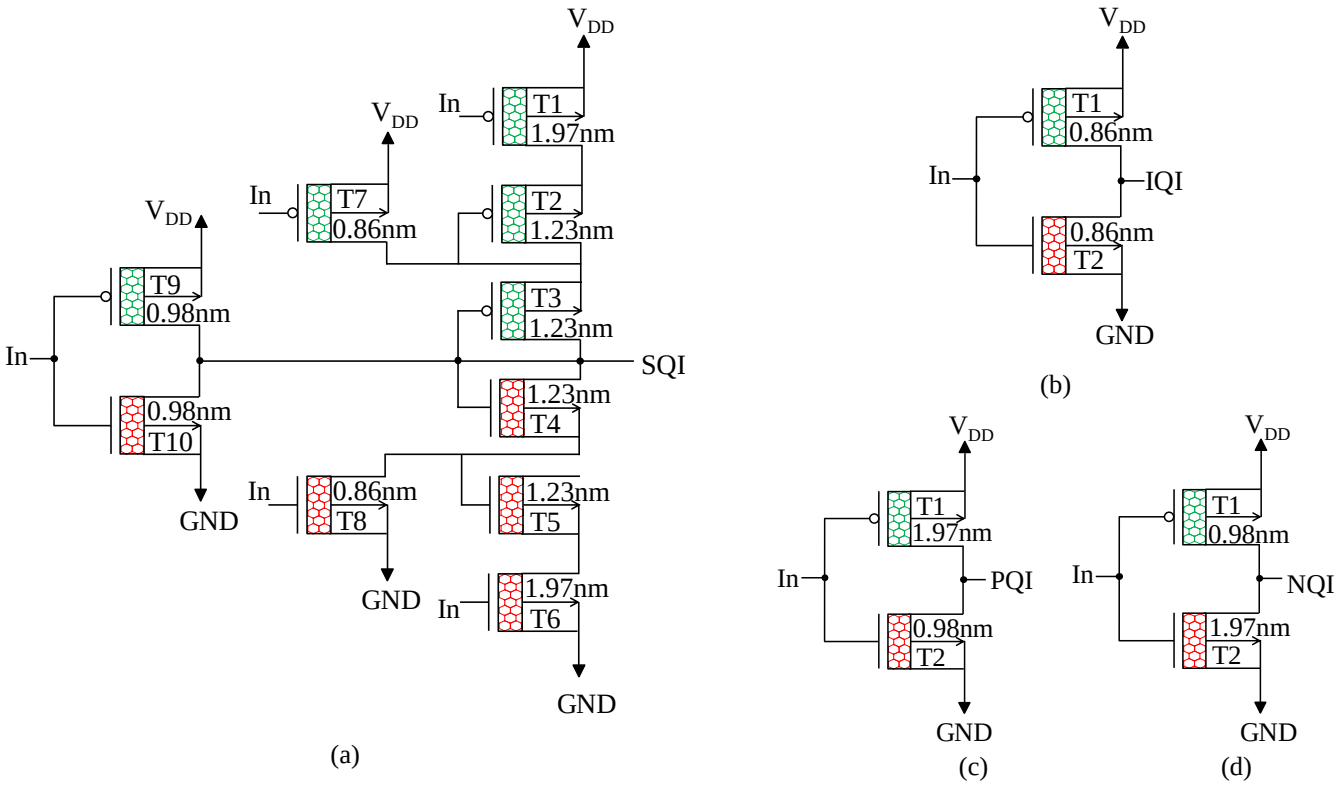

Fig. 9. GNRFET based (a) SQI, (b) IQI, (c) PQI, and (d) NQI.

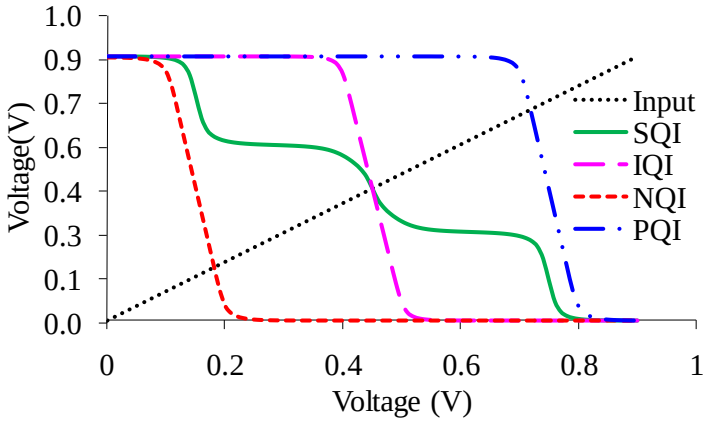

Fig. 10. Voltage transfer characteristic of proposed inverters.

4. 1 GNRFET based quaternary inverters

The SQI is developed utilizing ten GN based FETs and placed in Fig. 9 (a). The multiple threshold FETs are used by altering GN width. The V_{DD} value for the proposed circuits is used as 0.9V; hence the logic states 0, 1, 2 and 3 represent the voltages 0V, 0.3V, 0.6V and 0.9V, respectively. The *m* values 6, 7, 9 and 15 are considered for the transistors placement in the SPICE model. The width of transistor for 6, 7, 9 and

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15 are calculated as 0.86nm, 0.98nm, 1.23nm and 1.97nm, respectively, and the threshold values are 0.43V, 0.56V, 0.30V and 0.19V, respectively. For p-GNRFETs, the threshold values are -0.43V, -0.56V, -0.30V and -0.19V, respectively.

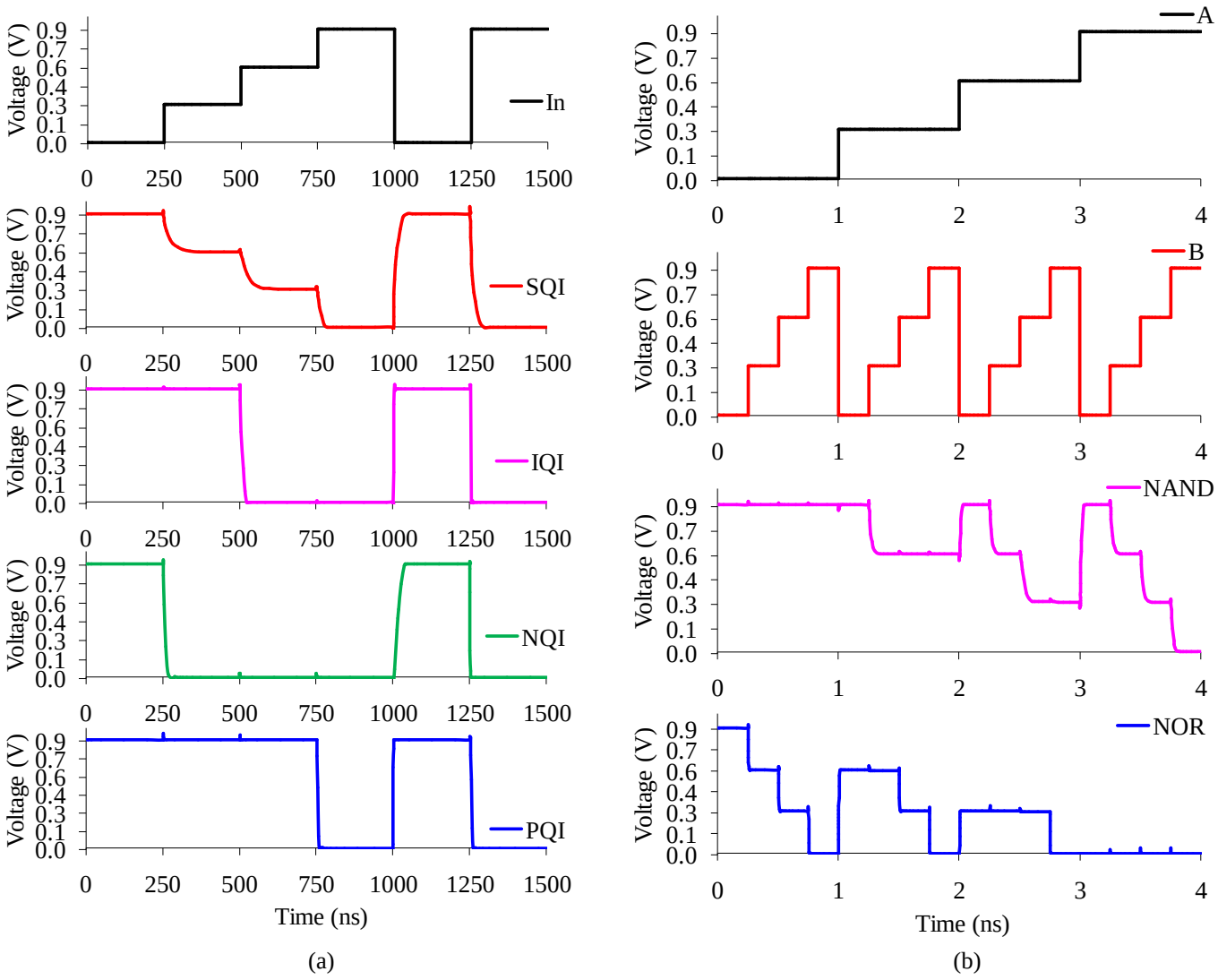

Fig. 11. Output responses of proposed circuits (a) Inverters and (b) Universal gates.

In the GNRFET based SQI, when the input value is '0', the GNRFETs T1, T7 and T9 are switched ON while the GNRFETs T6, T8 and T10 are switched OFF, and the output becomes '3'. After altering the input to '1', the GNRFETs T9 is switched OFF and T6 is switched ON and the other GNRFETs will be previous states. Hence, voltage division occurs and the output will change to logic '2'. When input is '2', the T7 is switched OFF and T8 is turned ON and the output becomes logic '1' because of the voltage division. When the input is logic '3', all the NGNRFETs are turned and PGNRFETs are turned OFF; thus,

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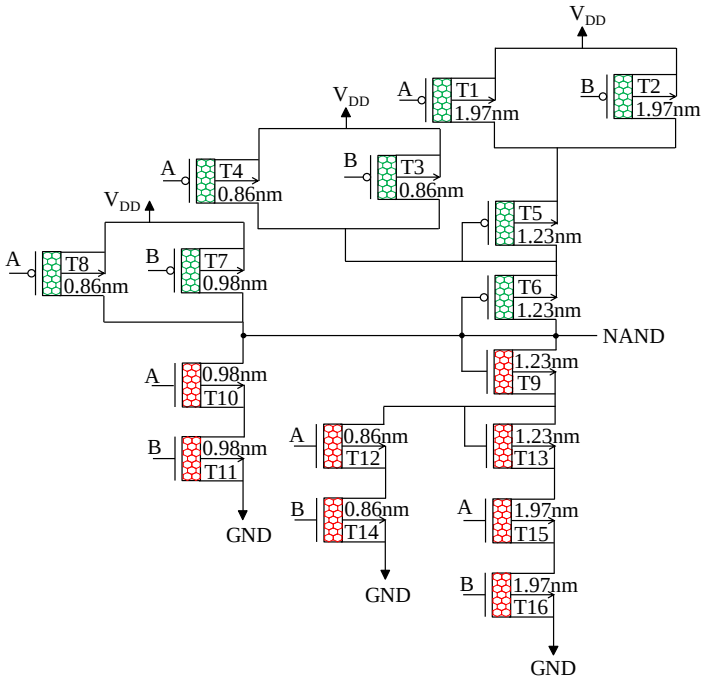
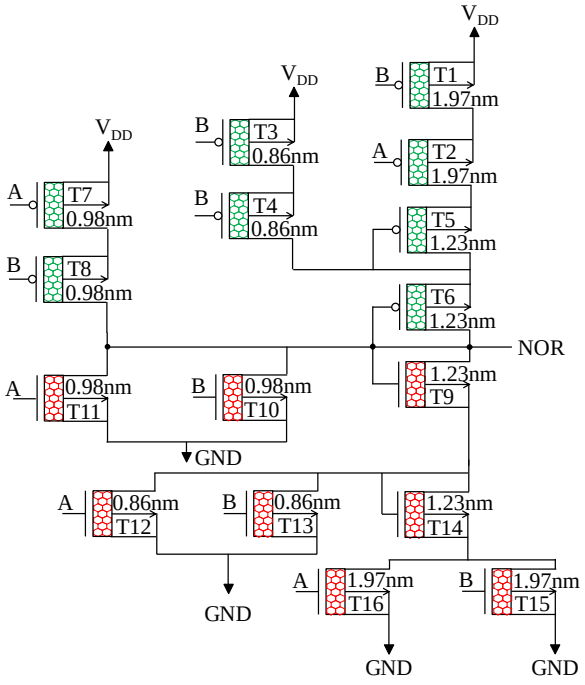
the output drops from logic '1' to logic '0'. Fig. 10 shows the VTC of the proposed SQI circuit. The input time of transition from low to high is adopted to be similar as the transition from low to high. The input and output waveforms of the proposed GNRFET based SQI obtained using HSPICE are shown in Fig. 11 (a). Additionally, the values of delay propagated and power dissipated for the proposed SQI is analyzed. The obtained average delay is 7.54E-12s and power dissipation is 0.48E-06W for the proposed SQI.

The proposed GNRFET based IQI circuit placed in Fig. 9 (b). In IQI circuit, the threshold value for T1 is 0.43V and T2 is -0.43V. When the input values are '0' and '1', the GNRFET T1 is turned ON and output value becomes the '3'. For the input values '2' and '3', the GNRFET T2 is switched ON and output value changes from '3' to '0'. The circuit schematic of GNRFET based PQI is shown in Fig. 9 (c). The threshold value of T1 is -0.19V and T2 is 0.56V. The output of PQI is '3' for the input values '0', '1' and '2' because the GNRFET T1 is turned ON. While the output value is '0' for the input '3' because of the GNRFET T2 is turned ON. The circuit of GNRFET based NQI is shown in Fig. 9 (d). In NQI, the threshold values are 0.56V and -0.19V for T1 and T2. The output of NQI is '3' for the input value '0' because the T1 is turned ON. While the output value is '0' for the input '1', '2', '3' because T2 is turned ON. The VTC and the output responses of proposed IQI, PQI and NQI circuits are shown in Fig. 10 and Fig. 11 (a), respectively. For IQI, PQI and NQI circuits, the obtained average delays are 2.52E-12s, 2.52E-12s, and 2.53E-12s and obtained power dissipations are 2.40E-07W, 4.09E-07W, and 8.83E-07W, respectively.



(a)



(b)

Fig. 12. GNRFET based (a) NAND gate and (b) NOR gate.

4.2 GNRFET based quaternary NAND and NOR gates

The circuit diagrams of universal NAND and NOR gates are placed in Fig. 12. The configurations of these gates consist of 16 GNRFETs with various GN widths 0.86nm, 0.98nm, 1.23nm and 1.97nm and the threshold values 0.43V, 0.56V, 0.30V and 0.19V, respectively. The waveforms of these circuits are shown in Fig. 11 (b).

4.3 GNRFET based quaternary half adder circuit

The above discussed quaternary logic designs are used to develop quaternary half adder circuit. The similar process can be employed to develop the other circuits like multipliers and subtractors, etc. The quaternary half adder numerical equations for sum and carry are given in (6). To define the each input value in the half adder, a decoder circuit is required which is placed in Fig. 7. The circuit schematic of quaternary half adder sum and carry circuits are shown in Fig. 13 (a) and Fig. 13 (b), respectively. The proposed quaternary half adder sum schematic consists 37 GNRFETs while the carry circuit consists 15 GNRFETs. The output of the half adder is given in Fig. 13 (c) and verified the responses with Table IV. The average delay, power and PDP obtained for GNRFET adder are given in Table VI.

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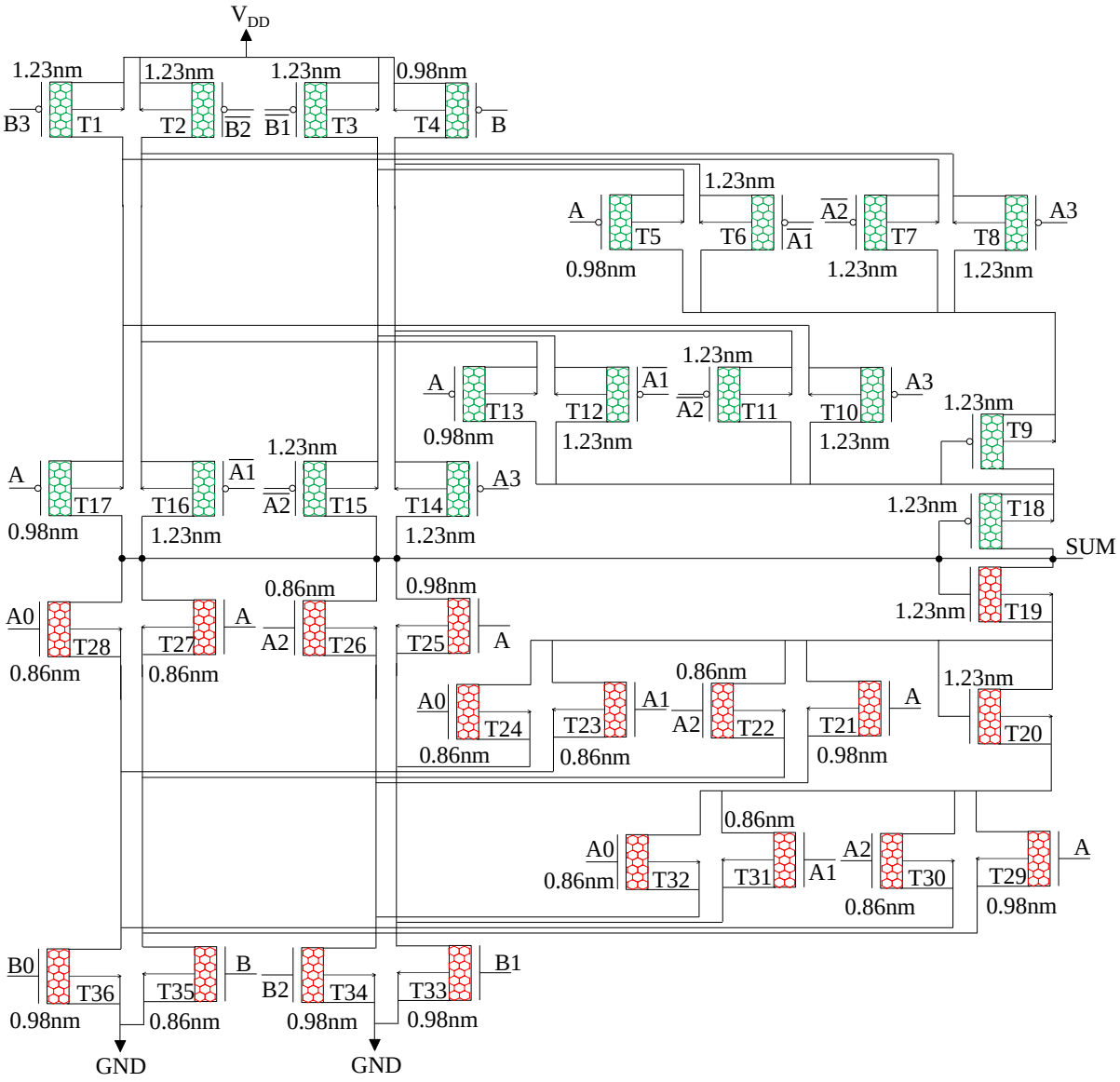

(a)

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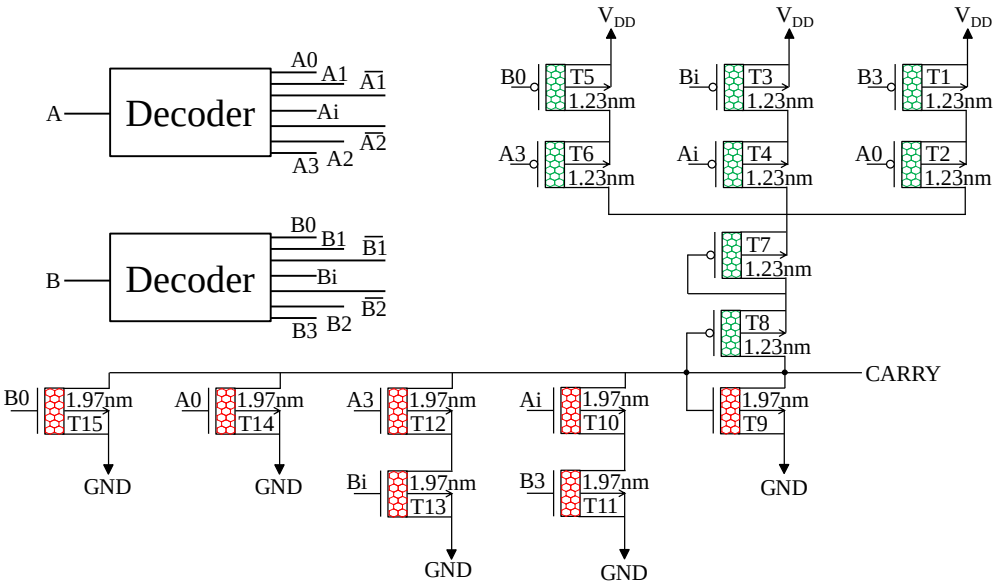
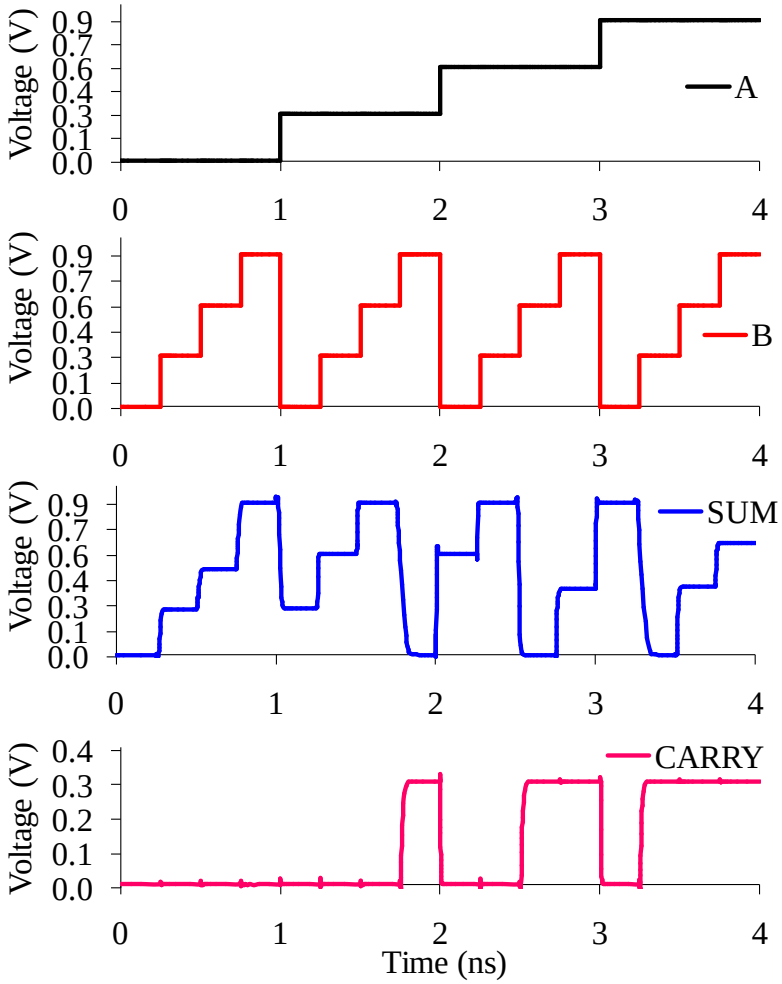


(b)



(c)

Fig. 13. Half adder (a) Sum circuit and (b) Carry circuit and (c) Output response

4.4 Comparison of GNRFET circuits with CNTFET based circuits

The proposed quaternary circuit's performance is compared to the CNTFET circuits. In CNTFETs, the threshold values are changed by varying the diameter CNT. Four CNT diameters 0.62nm, 1.02nm, 1.49nm, and 2.27nm are utilized and the corresponding threshold values are 0.68V, 0.42V, 0.29V, 0.19V, respectively. Depending on the multi-threshold CNTFETs, the quaternary logic circuits are designed using the model presented in [18, 19]. Table VI shows the delay, power dissipation and PDP for the GNRFET circuits and its comparison with CNTFET circuits. From the analysis, it is noticed that the GNRFET quaternary circuits show an improved delay, power, and PDP over the CNTFET based circuits.

Table VI
Performance comparison for both GNRFET and CNTFET based circuits

Parameters	GNRFET					CNTFET				
	SQI	IQI	NQI	PQI	Half adder	SQI	IQI	NQI	PQI	Half adder
Propagation Delay (ps)	7.54	2.52	2.53	2.52	192.29	11.67	5.09	5.24	5.24	298.09
Power Dissipation (μW)	0.48	0.24	0.88	0.40	20.30	0.72	0.43	0.72	0.39	45.36
Power Delay Product (fJ)	0.0036	0.0006	0.0022	0.0010	3.90	0.0084	0.0021	0.0037	0.0020	13.52

It is worth noting that research and development efforts are ongoing in the field of MVL, and there may be specific applications where it has found niche usage. However, overcoming the challenges such as compatibility, standardization, manufacturing and performance trade-offs, along with the considerable investment required for a large-scale transition, has prevented MVL from replacing binary logic in mainstream digital systems so far.

5. Conclusion

A new technique is presented to design the quaternary circuits by using the GNRFETs. The GNRFET threshold voltage is a function of GN dimer line value. Depending on this study, the multiple threshold GNRFETs are presented. The quaternary inverters and gates are developed using the GNRFETs. Then the quaternary half adder circuit is proposed as an extension. All the proposed quaternary designs are designed and simulated in the industry standard HSPICE simulator. The results of the proposed quaternary GNRFET designs are compared to conventional CNTFET designs. The comparison results confirmed that the quaternary GNRFET based SQI, IQI, PQI, NQI and half adder circuits achieve propagation delay, power dissipation and PDP improvements up to 36.25%, 53.17% and 71.11%, respectively over the CNTFETs. Hence, the proposed GNRFETs based implementations plays as important role in developing quaternary designs at both gate and circuit levels.

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