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OPTIMIZING STORED ENERGY IN SWITCHED-CAPACITORS FOR A FIVE-LEVEL X-TYPE BOOSTING INVERTER

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ABSTRACT— In this short, a unique five-level (5L) common ground type (CGT) inverter with dual voltage boosting capability based on switching capacitors (SCs) is proposed. Using a capacitor rated for peak output voltage is unavoidable in standard 5L CGTs, which has a detrimental effect on the power density of the inverter. Because the SCs in the suggested architecture are rated for half of the peak output voltage, there is less need for energy storage and a smaller voltage diversity factor. Furthermore, the suggested inverter can continue to function with lower power levels in the event that any capacitors fail. The suggested architecture also has sensorless operation, low dv/dt, and SC selfvoltage balancing. The suggested inverter's working concept and circuit description are explained in depth. To highlight the unique characteristics of the suggested inverter, a comparison of the state-of-the-art CGT topologies with the proposed inverter is provided. Lastly, simulation tests are used to verify the functioning and viability of the suggested inverter, and the outcomes are shown for both standalone and grid-connected operation.

Index Terms—Boosting, common-ground type, leakage current, switched capacitor (SCs), transformer-less multi-level inverter.

I.INTRODUCTION

Recently, multilevel inverters (MLIs) are widespread in photovoltaic (PV) applications due to their merits like better power quality, reduced harmonic distortion and low dv/dt. The MLIs are broadly classified into transformers-based and transformer-less. The latter is popular due to its compact, high efficient and economical features [1]–[3].

The major concerns in transformer-less MLIs (TLMLIs) is the flow of ground leakage current due to the parasitic capacitance between PV cells and the grounded metallic frame of each module and the need for additional boosting circuit [4]. Therefore, several TLMLIs topologies are specifically developed for reducing the leakage current and eliminating the high-frequency voltages across the parasitic capacitances. In addition, the concept of the amalgamation of switched capacitors (SCs) provides the voltage boosting ability [5]–[7]. Among all the available solutions, the topologies based on common ground type (CGT) eliminates the leakage current due to a solid connection between the PV negative terminal and grid/load neutral.

On this line, several CGT topologies with a voltage boosting gain of two are witnessed [8]–[12]. Despite having fewer switches, the topology presented in [8] has limitations on the achievable modulation and power factor. Topology in [9] has a higher total SC voltage (TSCV), which increases the stored energy and size. The topologies presented in [10]–[12] have a higher total standing voltage (TSV) and TSCV, which escalates

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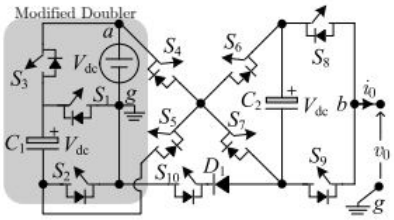

Fig. 1. Proposed X-type 5L boosting inverter topology.

cost and reduces the reliability of the inverter. Some of the major setbacks in the available topologies are the requirement of higher number of components, higher TSV, limited modulation index and restricted reactive power supplying ability. In addition, the conventional five-level (5L) CGTs must employ an SC rated for peak output voltage to generate negative output voltage levels, which inevitably requires high voltage rated semiconductor devices. Furthermore, SC failure results in complete shut down of the inverter due to the absence of redundant switching states for generation of negative voltage levels. Thus, the number of SCs and their voltage rating plays a significant role in determining the inverter's reliability [13]. In the literature, effort towards improving the CGT inverters reliability through reducing the energy stored in SCs has received a lesser attention.

In order to ameliorate the aforementioned drawbacks, moderate efforts are witnessed [14], [15]. However, topologies in [14], [15] suffers due to the over-usage of SC, resulting in higher ripple voltage. Therefore, this brief proposes a CGT inverter that achieves the twin objectives of reducing the stored energy of SCs and the ability to sustain SC failure. The prominent features of the proposed topology are as follows.

1) Has two SCs rated for only half of peak output voltage.

2) Lower TSV.

3) The maximum dv/dt across the semiconductor devices is within the input DC voltage (Vdc).

4) The SCs are self-voltage balanced.

5) Seven out of ten switches operate at near fundamental frequency (50 Hz), resulting in reduced switching losses.

A detailed comparative study is presented to highlights the superior features of the proposed topology over its counterparts. The operational feasibility is validated through several experimental test and the results are presented.

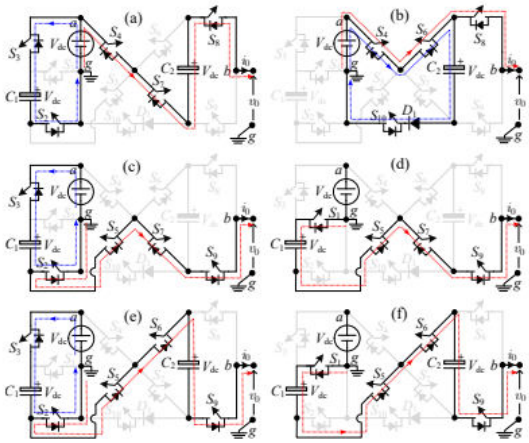

Fig. 2. Operating states and current conducting path (a) state A (b) state B (c)state C (d) state D (e) state E (f) state F.

II.DC-DC CONVERTERS

A DC-DC converter with a high step-up voltage, which can be used in various applications like automobile headlights, fuel cell energy conversion systems, solar-cell energy conversion systems and battery backup systems for uninterruptable power supplies.Theoritically, a dc-dc boost converter can attain a high step-up voltage with a high effective duty ratio.But,in practical, the step-up voltage gain is restricted by the effect of power switches and the equivalent series

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resistance(ESR) of inductors and capacitors.

Generally a conventional boost converter is used to get a high-step-up voltage gain with a large duty ratio. But, the efficiency and the voltage gain are restricted due to the losses of power switches and diodes, the equivalent series resistance of inductors and capacitors and the reverse recovery problem of diodes. Due to the leakage inductance of the transformer, high voltage stress and power dissipation effected by the active switch of these converters. To reduce the Voltage spike, a resistor-capacitor –diode snubbed can be employed to limit the voltage stress on the active switch. But, these results in reduction of effiency.Based on the coupled inductor; converters with low input ripple current are developed. The low input current ripple of these converters is realized by using an additional LC circuit with a coupled inductor.

Power engineering is the method used to supply electrical energy from a source to its users. It is of vital importance to industry. It is likely that the air we breathe and water we drink are taken for granted until they are not there.

III. MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure 4.1. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 4.2. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the

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Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \text{ where } n = 1,3,5,7 \ldots$$

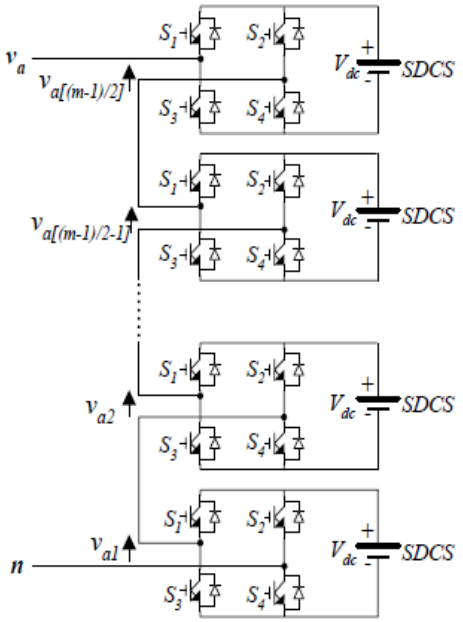

Fig3.Single-phase structure of a multilevel cascaded H-bridges inverter

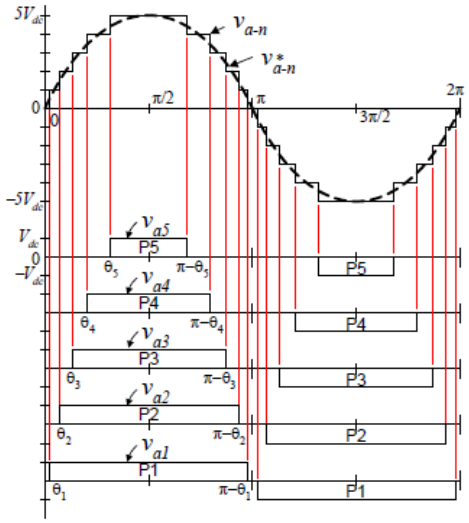

Fig4. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

IV.PROJECT DESCRIPTION AND CONTROL DESIGN

PROPOSED 5L CGT INVERTER

A. Motivation for the Proposed Topology

The voltage doubler unit forms an integrated part of 5L CGT topologies with dual voltage gain. With respect to the negative dc bus, the conventional voltage doubler can only generate positive voltage levels. Hence, an SC must be dedicated to creating a negative supply voltage for the inverter during the negative cycle and therefore needs to be charged to the peak output voltage, thus reducing power density and increasing the energy storage requirements. This paper proposes a modified voltage doubler circuit to synthesize the negative supply voltage with a reduced voltage across the SCs. This improved feature is achieved by the circuit configuration shown in Fig. 1. The proposed inverter generates a 5L voltage waveform using ten switches, a diode, and two SCs. At first glance, the usage of ten switches looks inconspicuous; however, its carefully arrangement aids in tackling the capacitor failures and sustaining operation. The devised structure has no restrictions or limitations with regard to the achievable modulation index and can operate for any arbitrary power factor.

B. Operating principle

The active switches, load current path, and status of SCs are detailed below

a) State A: The power switches S2, S3, S4, S7, S8 are ON, and other switches are OFF. As a result, the inverter output voltage v0 = Vdc + VC2 = 2Vdc, while C1 is charged to Vdc, as depicted in Fig. 2(a).

b) State B: The power switches S4, S6, S8, S10 are ON, and other switches are OFF. As a result, the inverter output voltage v0 = Vdc, while C2 charges at Vdc through S10 and D1, as depicted in Fig. 2(b).

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c) State C: The power switches S2, S3, S5, S7, S9 are ON, and other switches are OFF. As a result, the inverter output voltage, v0 = 0, while C1 charges to Vdc through S3, as depicted in Fig. 2(c).

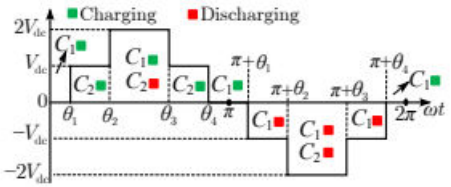

Fig. 5. SCs status with 5L fundamental waveform

d) State D: The power switches S1, S5, S7, S9 are ON, and other switches are OFF. As a result, the inverter output voltagev0 = -VC1 = -Vdc, as depicted in Fig. 2(d).

e) State E: The power switches S2, S3, S5, S6, S9 are ON, and other switches are OFF. As a result, the inverter output voltage is v0 = -VC2 = -Vdc, while C1 is charged to Vdc through switches S2 and S3, as depicted in Fig. 2(e).

f) State F: The power switches S1, S5, S6, S9 are ON, and other switches are OFF. As a result, the inverter output voltage is v0 = -VC1 - VC2 = -2Vdc as depicted in Fig. 2(f).

From the above states, the availability of the redundant states enables the proposed inverter to sustain the operation with a reduced number of voltage levels (three) during the event of a capacitor failure. This unique feature makes the proposed topology distinctive from the conventional 5L CGTs available till date, which are highly vulnerable to SC failures. Further, the charging and discharging effects of switching states on the SC voltages are depicted in Fig. 3. According to Fig. 3, the maximum discharge interval (MDI) of C1 is $(\pi + \theta4)-(\pi + \theta1)$, and its capacitance is expressed as $C1 = 2Vdc\ R0\times\omega0\times\Delta vC1 \times (\theta4 - \theta1)$. Where $\Delta vC1$ is the ripple voltage of C1, $\omega0$ is the fundamental frequency, and the MDI of C2 is $\theta3-\theta2$ and the same process is used to determine the capacitance of C2.

COMPARATIVE ASSESSMENT

For a fair comparison, the proposed CGT inverter topology is compared to similar state-of-the-art topologies with a twofold voltage gain, SC voltage self-balancing capability, and a single input source. Table I illustrates the configurations, component count (Ncomp), and other figures of merit such as TSV, energy storage per unit (ESp.u.), gain, total SC voltage (TSCV), number of maximum conducting devices (NMCD) for a particular level, number of devices with maximum voltage stress (NDMVS) and efficiency (η), etc. Further, the key distinctive features of the proposed topology are reiterated.

a) Blocking Voltage of Semiconductor Devices and TSV: The maximum blocking voltage (MBV) is a key factor in the selection of semiconductor devices. Three switches and one diode in [8], five switches in [9] and four switches in [10], [12], [14], [15] has a MBV of v0,peak. Further, the blocking voltage of two switches in [10], [11] is greater than v0,peak. However, in the proposed topology, only one switch and a diode are required to block v0,peak, while the remaining switches block half of the v0,peak. As a result, TSV and power losses are reduced.

b) SC Voltage Rating and Total Stored Energy of Capacitors : The TSCV is the sum of the individual SC voltages, which indicates the volume of SCs, voltage diversity factor,

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TABLE I COMPARATIVE ANALYSIS OF THE PROPOSED TOPOLOGY WITH THE RECENT TWO-FOLD GAIN 5L SC-BASED CGT INVERTERS

TABLE II COST COMPARISON AND ASSESSMENT

Item	Part Number	Description	Cost ($)	[P]	[15]	[12]	[14]	[11]	[10]	[9]	[8]
	RCX220N25	250V,22A	2.02	9	4	5	5	2	2	2	3
A	IRFP460PBF	500V,20A	4.91	1	4	4	4	2	4	5	3
	UJ4C075060K3S	750V,28A	9.63	-	-	-	-	-	1	-	-
	IXFH20N100P-ND	1000V,20A	13.30	-	-	-	-	2	1	-	-
B	SDUR2030	300V, 20A	1.12	-	2	1	-	1	1	1	1
	BYC20-600,127	500V,20A	1.74	1	-	1	-	2	-	-	1
C	B43415C3218A000	2.1mF,300V	14.46	2	2	2	2	1	1	1	1
	ALF70G222KP500	2.2mF,500V	23.72	-	-	1	-	2	1	1	1
D	TLP250		2.18	10	8	7	8	6	6	7	6
		Total Cost ($)		75.5	76.3	100.5	76.1	120	100	83.2	74.9

A=Switches, B=Diodes, C=Capacitor D=Gate Driver P=Proposed ↑=Increase ↓=Decrease, The cost of items is mentioned by referring to www.digikey.com

and energy storage requirements. From Table I, for identical capacitance values across the considered topologies, the energy stored in [8]–[10], [11], [12] is 2.5, 4.5 and thrice that of the proposed topology. The topologies in [14], [15] and the proposed have an identical TSCVp.u. of unity.

c) Power Loss Analysis: The power loss analysis is carried out using the thermal models of the PLECS software. For the analysis, a 1 kW, 400 V system is considered equipped with the switches IKQ120N60T, diode MSC050SDA070B, ambient temperature 25◦C, unity power factor, and the same operating conditions for all of topologies under consideration. The obtained loss distribution is shown in Fig. 4. From the results, the proposed topology has a competent loss distribution over its other counterparts.

d) Case Study on the Inverter Cost: A comprehensive cost analysis is carried out with a safety factor of 25 % upon the device ratings. For a peak output voltage of 400 V and 1 kW power rating, the price analysis is summarised in Table II. Overall, from the cost point of view, topologies in [8], [14], [15] are in par to the proposed topology. The increased cost requirements of the other topologies are attributed to the higher number of SCs, switches, and their higher ratings. Some key figures of merit of the CGT inverters are consolidated in the radar chart depicted in Fig. 5. The smaller the spread area, the better the overall performance of a given inverter. From Fig. 5, it is evident that the proposed topology is dispersed over the smallest area, highlighting its novelty and superiority over its counterparts.

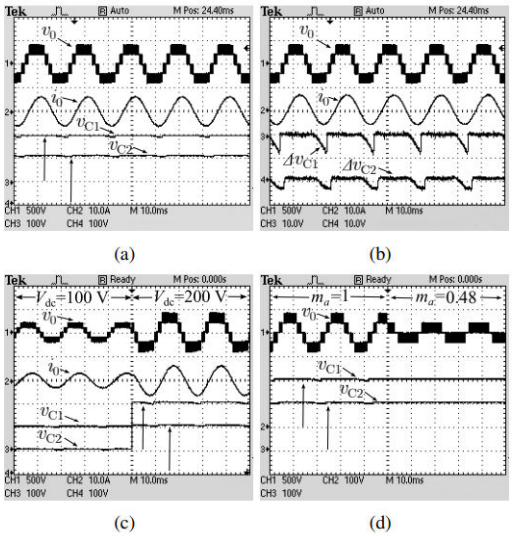

Fig. 6. results in stand-alone mode (a) v0, i0 and SC voltages (b) v0, i0 and SC voltage ripple with RL load under steady-state (c) v0, i0 and SC voltages when step change in input voltage from 100 V to 200 V (d) v0 and SCs voltages when step change in modulation index.

V.CONCLUSION

A 5L X-type CGT inverter with self-voltage balancing, voltage boosting, and fewer components was shown in this short. The dependability of the inverter is increased by the lower switching losses and capacitor energy stored as a result of the

decreased SC voltage rating, which also imposes lower voltage stress across the semiconductors. Furthermore, the suggested inverter can continue to function even in the event of a capacitor failure. The unique characteristics of the suggested topology were emphasised by a thorough quantitative and cost-based comparison. Lastly, taking into account the stand-alone and grid-connected case studies, the experimental findings confirmed the viability of the suggested architecture.

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