International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Implementation Of Internet Voting Machine Using Verilog HDL

N.Pandu Ranga[1], Dr.Damala Dayakar Rao[2]
Associate Professor[1,2]
Department of ECE
MREC

Abstract- Conventional paper based voting procedure was terribly long process and extremely prone to errors. Polling by Electronic Voting Machine (EVM) is easy, safe and secure methodology that takes minimum of our time .In order to perform this mechanism, there were several phases in the design process such as designing a flow chart, algorithm and simultaneously the code is developed to implement & stimulate the logic. The proposed digital EVM was designed on Xilinx ISE using verilog HDL and can also be implemented on FPGA board for real time purpose. The proposed method consists of 3 stages, in the first stage we decide the total no. of voters and the total number of contestants taking part in the election process .we have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In stage two, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry. In stage three after completion of voting process the votes are validated by comparing the votes polled to the contestants in their registries after which the election process ends by declaring the winner. The above proposed method can be implemented on FPGA board for real time applications ranging from university level elections to Assembly and LokSabha elections, as it has the advantage that it can be reprogrammed over and over for various tasks according to their requirement which helps in reducing the expenditure.

Index Terms- *HDL,XILINX,EVM,FPGA.*

I. INTRODUCTION

Casting a ballot is the sole criteria for picking their agents by individuals in any vote based system, along these lines, this whole procedure ought to be finished with most extreme consideration so just a reasonable and meriting hopeful is chosen that is exclusively founded on popular conclusion. In prior days, decisions were led utilizing poll paper framework whereby individuals threw their votes to their most well-liked challenger, just, by setting stamp against his/her name however this strategy regularly experienced different defects, for example, taking of votes and unjustifiable outcomes [5].

To defeat every one of these disparities, electronic casting a ballot machine was planned. Be that as it may, the plan of straightforward electronic casting a ballot machine with removable memory card was scarce as access to memory card for even an instant will alter all of the votes with some completely different malignant code. So we tend to need a frame work that might offer some better technique for executing Electronic Voting Machine.

Since we tend to understand that it is laborious to manage control signals, hence we have structured electronic casting a ballot machine in Verilog HDL utilizing Xilinx ISE 9.2i which can be actualized on FPGA (Field Programmable Gate Array) equipment. Further, this execution likewise contains secret key which itself is computerized in nature and is hard to be hacked.

II. LITERATURE SURVEY

Smith, T.F., Waterman, M.S [1] stated in their paper that Electronic mechanical device could be an easy device accustomed to record votes mechanically without the necessity of manual operation of ballot papers. Basic right to vote forms the premise of any Democracy. Altogether earlier elections, voters casted their votes to their favorite candidates by putt the stamp against his/her name. This is often a protracted time overwhelming method associated is at risk of errors and may every now and then be an unfair method.

May, P., Ehrlich, H.C., Steinke, T [2], illustrated in their paper that to overcome of these difficulties and build the electoral method a good one, implementation of electronic mechanical device in digital domain is given during this paper it's troublesome to tamper votes in digital domain and provides a secure and safe technique for conducting elections Czajkowski, K., Fitzgerald, S., Foster, I., Kesselman, C.[3], described in their paper that the traditional choice procedure was terribly long and long method and extremely a lot of liable to errors. Polling by Electronic mechanical device (EVM) may be a straightforward, safe and secure technique that takes minimum of your time. Current Electronic mechanical device (EVMs) utilized in LOK SABHA and an ASSEMBLY election accepts only 1 vote from every citizen. However in elections like GRAMA PANCHAYATH and COOPERATIVE SOCIETIES, wherever every citizen casts their votes to quite one candidate, offered choice machines won't work. The paper additionally

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

presents a PROGRAMMABLE ELECTRONIC mechanical device that accepts one or a lot of votes reckoning on demand. Mode management is enclosed in EVM, through that it's attainable to line the EVM to just accept over one vote from every elector reckoning on the sort of elections. the most advantage of this sort of EVM is to avoid the invalid votes particularly in co-operative society elections wherever every elector has got to forged vote for 9 candidates.

Foster, I., Kesselman, C., Nick, J., Tuecke, S[4], stated in their paper that in previous couple of years, Secured physical science mechanical device exploitation Biometric was enforced. In this machine, advanced engineering is employed. This method employs that replace incident and most significant error prone human part. It will increase flexibility and avoids false choice. To evidence a vote, elector must use fingerprint. Thus vote is exclusive.

III. PROPOSED WORK

Traditional paper primarily based option procedure was terribly long and long method and extremely abundant susceptible to errors. Polling by Electronic mechanical device (EVM) may be a straightforward, safe and secure methodology that takes minimum of your time. The proposed digital EVM was designed using Verilog HDL and implemented on Spartan 3 FPGA. The proposed method consists of 3 stages; in the first stage we decide the total no. of voters and the total number of contestants taking part in the election process. We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In stage two, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry. In stage three after completion of voting process the votes are validated by comparing the votes polled to the contestants with their registries after which the election process ends. The above proposed method can be implemented on FPGA as it has the advantage that it can be reprogrammed over and over for different tasks, making them very cost efficient by avoiding recurring expenses.

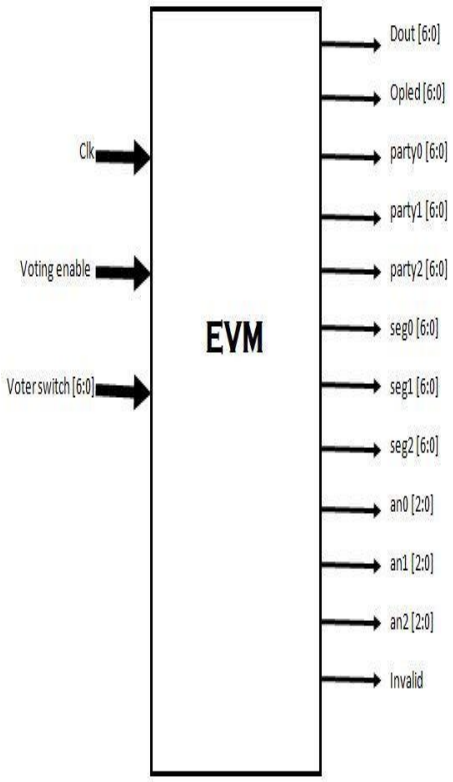
A. EVM Schematic

Fig. 1.EVM Schematic

The fig 1 shows the Schematic of proposed electronic voting machine with input and output signals.

The block diagram consists of clk, voting _enable and voter _switch as input signals. The dout, opled, party0, party1, party2, seg0, seg1, seg2, and invalid as output signals. The an0, an1, an2 are the intermediate signals which are used to enable the corresponding seven segment displays (seg0,seg1, seg2).

B. EVM Design and Implementation



International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

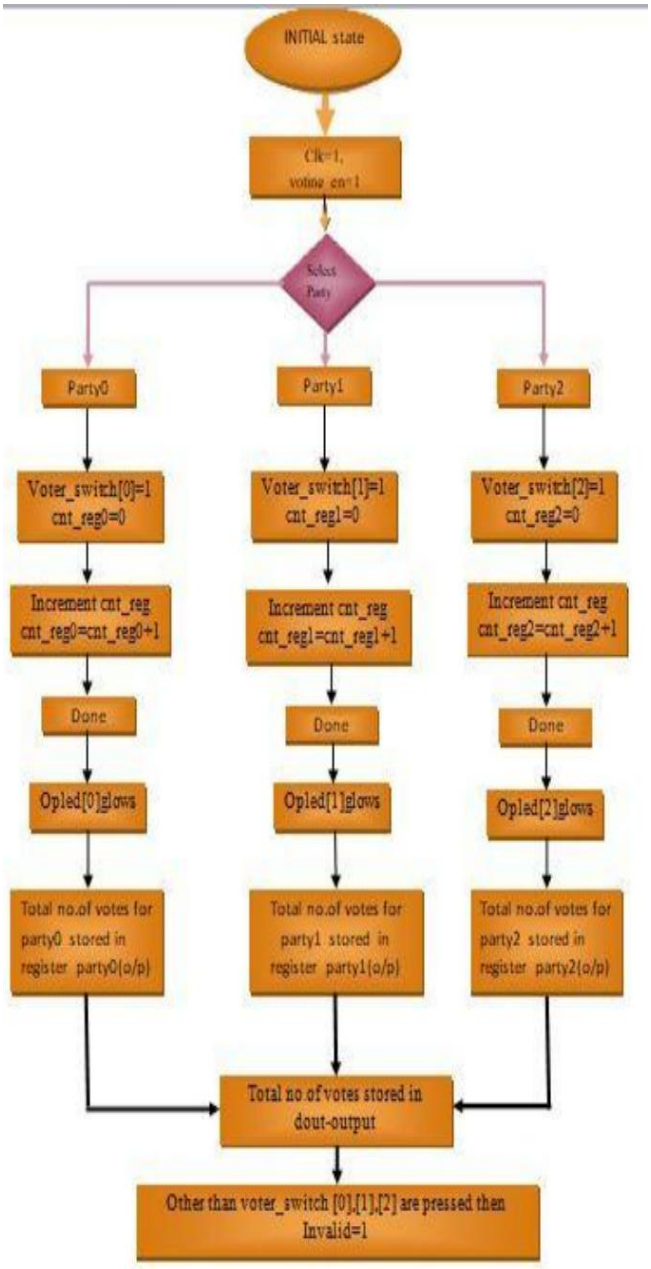


Fig 2: Flow Chart of Proposed EVM.

TABLE1. Description of Signals Used In Implementation.

Sno.	*SIGNAL*	*SIGNALTYPE*	*DESCRIPTION*
1	Clk	Input	Default clk is applied as input to the system
2	Voting _enable	Input	It is a active high signal which when enabled then the voting process begins.
3	Voter_switch	Input	This signal determines the total no. of parties participating in the electionprocess, in the present designit [3 down to 0] switch.
4	Opled	Output	This signal is high when the corresponding voter switch is enabled which helps to identify whether the vote is registered to a corresponding party or not.
5	Party0	Output	This register holds the total no. of votes polled to party0
6	Party1	Output	This register holds the total no. of votes polled to party1
7	Party2	Output	This register holds the total no. of votes polled to party2
8	Dout	Output	This register holds the total no. of votes polled in the entire election process of all the parties.
9	An0	Intermediate signal	This is active low signal used to activate seven segmentdisplay (seg0)
10	An1	Intermediate signal	This is active low signal usedto activate seven segmentdisplay (seg1)
11	An2	Intermediate signal	This is active low signal used to activate seven segmentdisplay (seg2)
12	Seg0	Output	This is seven segment display which displays the total no. of votes polled to party0
13	Seg1	Output	This is seven segment display which displays the total no. of votes polled to party1
14	Seg2	Output	This is seven segment display which displays the total no. of votes polled to party2
15	Invalid	Output	This signal is high whenever the invalid votes are polled.

The proposed digital EVM was designed (fig2) using verilog HDL and can be implemented on FPGA. The proposed method consists of 3 stages, in the first stage we decide the total no. of voters and the total number of contestants taking part in the election process.

We have assigned Voting enable which is active high input signal for the voter in order to cast his vote by using voter switch input signal for making this election process more secure and safe. In stage two, voting process begins when the voter casts his vote to a particular party or contestants the polled vote is registered in the individual contestant registry.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

In stage three after completion of voting process the votes are validated by comparing the votes polled to the contestants with their registries after which the election process ends.

The above proposed method can be implemented on FPGA as it has the advantage that it can be reinvented again and again for various undertakings, making them very cost effective by abstaining from repeating costs.

The proposed electronic voting machine with input and output signals like clk, voting _enable and voter_switch which act as input signals. The dout, opled, party0, party1, party2, seg0, seg1, seg2, and invalid will act as output signals. The an0, an1, an2 are the intermediate signals which are used to enable the corresponding seven segment displays (seg0, seg1, seg2).

The voting process in the first phase begins with the input clock signal (upto 100 MHz). At each positive edge of the clock signal the voting_en signal is synchronized. Voting_en is a active high signal which when enabled then the voting process begins. This signal plays a key role in election process because the vote casted by the voter is valid if and only if this voting_en signal is made high. So, this signal can be controlled by a polling officer at the polling booth. Voter_switch is another input signal used in our design. This signal determines the total no. of parties contesting in the election process, in the present design it [3 down to 0] switch. This signal allocates a switch to each party contesting in the election process.

In the proposed design we have taken three parties for contesting the election process. At the point when the voter is prepared to make his choice the surveying official ought to confirm whether the clock and voting_en the two signals are high, now the voter can cast his vote of his own choice by enabling the corresponding Voter_switch signal. Now, after casting the vote the output led of the corresponding party glows which indicate that his vote has been casted successfully.

In the present design we have allocated three led‟s to three parties who are contesting in the elections. So whenever the clock signal is high and Voting_en is high and say Voter_switch [0] is enabled the corresponding op led [0] glows. This process continues for the entire election process until the voting process concludes that is all the voters in that polling booth cast their votes to the parties of their choice.Now, once when the entire process completes, the dout register consists of the total no of valid votes polled in the election process. This helps in knowing the total votes polled. The party0, party1 and party2 registers will contain the votes polled to the corresponding parties individually in order to determine the winner.

In the proposed design we have used three seven segment displays (sego, seg1, seg2) which will display the contents of the party registers. So we have three seven segment displays which will display the contents of three parties (party0, party1, party2). To enable each seven segment display we used three active low anodes like an0, an1, an2 which when goes low enable the corresponding seven segment displays.

IV. RESULTS AND DISCUSSION(IF ANY)

The RTL schematic shows (Fig 3) the inputs and outputs of the evm module. The inputs to the module are voter_switch, clk, voting_en and the outputs of the module are an0, an1, an2, dout, output led, party0, party1, and party2, invalid, seg0, seg1 and seg2.

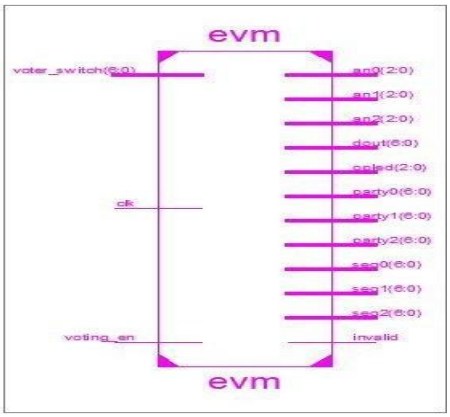


Fig3: RTL Schematic view

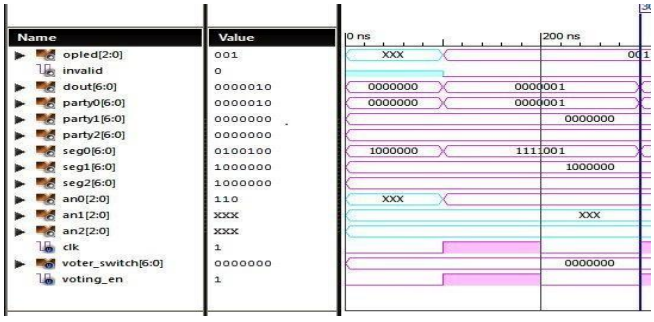


Fig 4: output waveform when for first vote is casted.

From the above figure 4 we can observe that when clk=1 and voting_en=1, vote is casted for party0 and hence the corresponding opled [0] is set high and segment0 displays a “one” value in seven segment.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

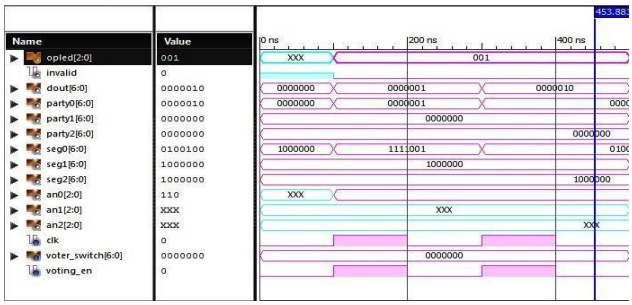


Fig 5: output waveform after second vote is casted

From the above figure 5 we can observe that when clk=1 and voting_en=1, again the vote is casted for party0 and hence the corresponding opled [0] is set high and segment0 displays a "two" value in seven segment.

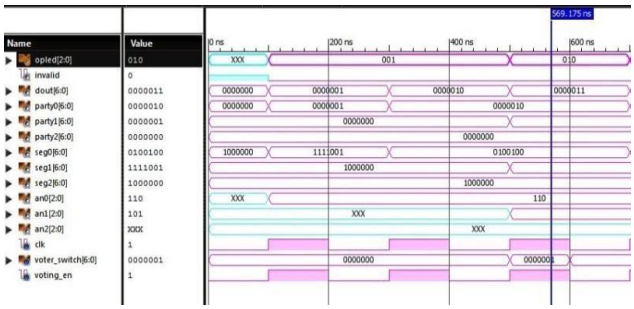


Fig 6: output waveform after third vote is casted

From the above figure 6 we can observe that when clk=1 and voting_en=1, now the vote is casted for party1 and hence the corresponding opled [1] is set high and segment1 displays a "one" value in seven segment.

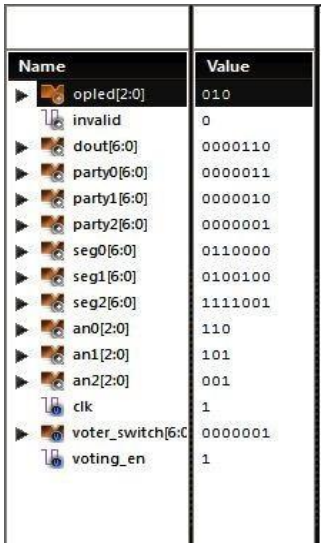


Fig 7: Result after all votes have been casted.

From the above figure 7 we can conclude that after the election process has completed the dout register shows the total no.of votes casted (here it is 6 votes).out of which party0 register shows three votes ,party1 shows 2 votes and party1 shows one vote, correspondingly the seven segment display shows the total no.of votes obtained by party0, party1 and party2.With this information we can declare , that the party0 has won the election and since the invalid output is low which indicates that there are no invalid votes in the entire election process.

Fig 8: final output at the end of election process.

V. CONCLUSION

The Xilinx based electronic voting machine met the requirements of the election process such as Enrolling the total no.of voters & contestants in the first stage, allowing the voter to cast his vote to a particular party of his choice which in turn is confirmed by the opled in the second stage. In the final stage it compares all the valid votes polled to different parties and confirm the winner of the election. We hereby conclude that the simulated design can be readily implemented on any FPGA board. Future Enhancement of this project involves the security section of the EVM. The security section of the EVM is one of the main parts of the project where each voter will hold an individual voting card and his or her finger print will be the password. The computer will scan the identity of the voter and then the polling officer will allow the voter to cast his,/her vote if found eligible. Our design can also be enhanced to the PRSTV Election process which is generally used in President, Vice President and Vidhana Parishad Elections in which the voter will cast more than one vote .

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

REFERENCES

1. Smith, T.F., Waterman, M.S.: Identification of Common Molecular Subsequences. J. Mol. Biol. 147, 195–197 (1981) .
2. May, P., Ehrlich, H.C., Steinke, T.: ZIB Structure Prediction Pipeline: Composing a Complex Biological Workflow through Web Services. In: Nagel, W.E., Walter, W.V., Lehner, W. (eds.) Euro-Par 2006. LNCS, vol. 4128, pp. 1148–1158. Springer, Heidelberg (2006)
3. Czajkowski, K., Fitzgerald, S., Foster, I., Kesselman, C.: Grid Information Services for Distributed Resource Sharing. In: 10th IEEE International Symposium on High Performance Distributed Computing, pp. 181–184. IEEE Press, New York (2001)
4. Foster, I., Kesselman, C., Nick, J., Tuecke, S.: The Physiology of the Grid: an Open Grid Services Architecture for Distributed Systems Integration. Technical report, Global Grid Forum (2002) .
5. N.S.N. LAKSHMI PATHI RAJU, A.PRAVIN, N.S.MURTHY SHARMA, S.S.KIRAN A Novel Proposal On Implementation Of Polling Percentage Improvement System Through Embedded Based Integration Of electronic Voting Machine And Other Methodologies – IJ ETA ETS ISSN: 0974-3588 | JULY ‟12 – DECEMBER ‟12 | Volume 5 : Issue 2 pp 1-5
6. Davide Balzarotti, Greg Banks, Marco Cova,"An Experience in Testing the Security of Real-World Electronic Voting Systems" IEEE Transactions On Software Engineering, Vol. 36, No. 4, July/August 2010
7. Sahibzada Muhammad Ali, Chaudhary Arshad Mehmood,Ahsan Khawja, "Micro-Controller Based Smart Electronic Voting Machine System" IEEE Conference 21-22 March 2013
8. D. Ashok Kumar and T. Ummal Sariba Begum "Electronic voting machine — A review" Pattern Recognition, Informatics and Medical Engineering (PRIME), 2012,IEEE Conference 21-23 March 2012
9. Hari K. Prasad , J. Alex Halderman , Rop Gonggrijp , "Security Analysis of India's Electronic Voting Machines" appeared in Proc. 17th ACM Conference on Computer and Communications Security , July 2010