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High-speed low-power voltage level converter based on adjustable pull-up cross-coupling network

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Abstract— In this brief, a fast and very low power voltage level shifter (LS) is presented. By using a new regulated cross-coupled (RCC) pull-up network, the switching speed is boosted and the dynamic power consumption is highly reduced. The proposed (LS) has the ability to convert input signals with voltage levels much lower than the threshold voltage of a MOS device to higher nominal supply voltage levels. The presented LS occupies a small silicon area owing to its very low number of elements and is ultra-low-power, making it suitable for low-power applications such as implantable medical devices and wireless sensor networks. Results of the post-layout simulation in a standard 0.18-µm CMOS technology show that the proposed circuit can convert up input voltage levels as low as 80 mV. The power dissipation and propagation delay of the proposed level shifter for a low/high supply voltages of 0.4/1.8 V and input frequency of 1 MHz are 123.1 nW and 23.7 ns, respectively.

Index Terms— Dual-supply, level shifter, differential cascade voltage switch (DCVS), subthreshold circuit, low-power

I. INTRODUCTION:

The efficient and very low power voltage level shifter is briefly discussed in the paper, theswitching speed is increased day by day in analog and digital signal processing applications while the dynamic power consumption also decreased by adopting a new regulated cross coupled method of pull up network. The proposed level shifter may transform input signal with voltage levels far lower than a MOS device threshold voltage to greater nominal supply voltage levels. Even though to low number of components, the proposed level shifter method occupies a tiny silicon area with ultra low power consumptions by making it appropriate low power applications such as implanted medical devices and wireless sensor networks. the results of this work analyzed in Tanner EDA tool at 180 nm and 45 nm CMOS technology. The power dissipation and propagation delay of the proposed level shifter are 1.173 mW respectively, for low / high supply voltage of 0.4/1.8V and input frequency of 1 MHz .

The schematic of the proposed level shifter is shown in Fig. 1. Our design is a modified DCVS structure, which includes a new regulated cross-

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coupled (RCC) pair for pull-up part. The proposed technique regulates the strength of the pull-up network and reduces the charge or discharge time of the critical internal nodes, which consequently increases the switching speed and reduces the dynamic power dissipation. For a better understanding of the proposed LS, the operation of the circuit for a low-to-high transition is shown in Fig. 2, in three steps.

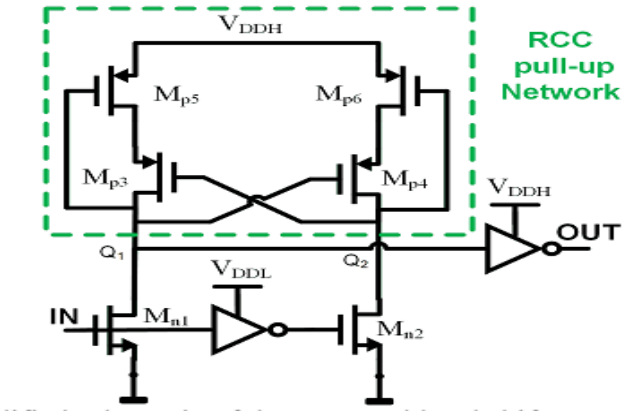

Figure 1 : Simplified schematic of the proposed level shifter

At the initial moment, the voltage of the node Q1 is high at VH (which is normally less than VDDH) whereas the voltage of Q2 is low. Hence, the Mp3 and Mp6 are on and the Mp4 and Mp5 are off. At first step, a low-to-high input transition causes Mn1 to switch on and Mn2 to switch off. So, the parasitic capacitors in the Q1 node begin to discharge and since the pull-up current through Mp3 is quite low by Mp5, node Q1 is discharged very fast. This condition continues until Vth where Mp4 and Mp5–Q1 reaches approximately to VDDH begin to turn on. Thus, at second step, as Mp4 turns on, Q2 voltage starts to increase and causes Mp3 and Mp6 to turn off gradually. In this step, the regenerative process of the pull-up network is enabled and makes the voltage of Q2 to increase very fast. Obviously, Mp6 is turned off before Q2 reaches VDDH and thus Q2 stays at VH. Thus, the maximum voltage level in the intermediate nodes (Q1 and Q2) is always less than VDDH, which helps reduce dynamic power. It is worth noting that the transistors in the pull-up network never turn off completely always entering deep sub threshold region as their gate-source voltage acquires the difference of VDDH and VH. This fact helps the transistors in the pull-up network to change state more quickly further increasing the circuit speed.

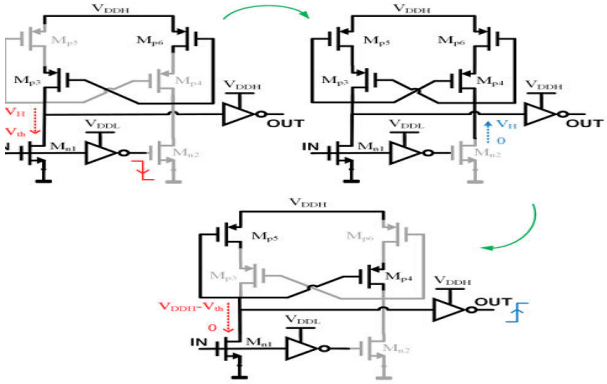

Figure 2 Operation of the proposed LS for L→H transition

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In prior researches, different LS architectures have been introduced to overcome the constraints of the conventional LSs operating in sub threshold region. The topology presented tries to reduce low-to-high transition delay using a level shifting capacitor frequently charged to VDDH and VDDL differences. When pulling down the output node, the current of the pull-up device is reduced while the pull-down device is strengthened using an auxiliary circuit, resulting in higher conversion speed. The suggested LS is a hybrid structure that contains generic CMOS logic gates and the modified Wilson current mirror to increase the voltage conversion range. The circuits presented to utilize a self-controlled current limiter to reduce static power. The architecture of two-stage conventional comparator to generate the output levels. The topologies presented are based on DCVS architecture, it has been tried to decrease the strength of the pull up device by limiting their currents. A self-adapting pull-up network and a split-input inverting buffer are utilized in for increasing the switching speed and reducing the dynamic energy consumption.

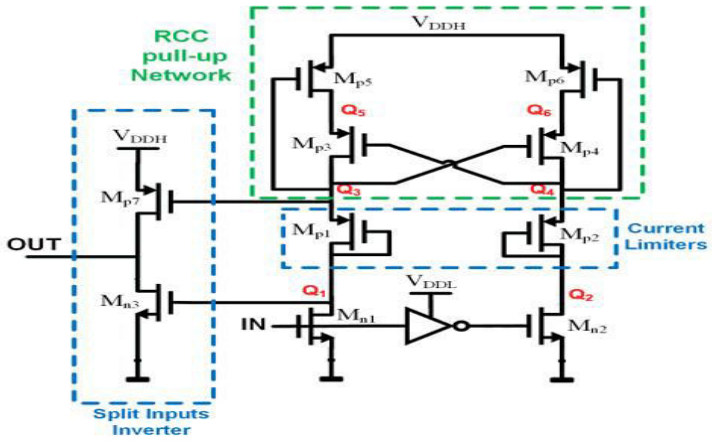

Figure 3 : . Schematic of the complete proposed level shifter.

Advantages :

- Less power consumption
- High speed system
- Single power supply to control over all circuit
- Increasing switching speed and dynamic energy consumption

II LITERATURE REVIEW

T A System of Two Coupled Oscillators With a Continuously Controllable Phase Shift. Vahnood Pourahmad , Farzad Khoeini, and Ehsan Afshari ,1549-8328 2018 IEEE. We present a novel generalization of quadrature oscillators (QVCO) which we call “arbitrary phase oscillator” or APO for short. In contrast to a QVCO which generates only quadrature phases, the APO is capable of continuously generating any desired phase at its output. The proposed structure employs a novel coupling mechanism to generate arbitrary phase shifts between two coupled oscillators without the need for an explicit phase shifter. A rigorous nonlinear dynamic

analysis is presented to give a closed-form formula for the generated phase shifts, and the theory is verified by numerical simulation as well as measurement results of a prototype chip fabricated in 130-nm CMOS technology. The prototype APO has a frequency tuning range of 4.90–5.65 GHz and is continuously phase tunable from 0◦ to 360◦ across the entire frequency range. The APO structure can be used in designing novel coupled-oscillator-based phased arrays for 5G wireless communications.

Multiphase LC OscillatorsLuca Romanò, Salvatore Levantino, Carlo Samori and Andrea L. Lacaita ,1057-7122 2006 IEEEThis paper proposes an extensive analysis of multiphase LC oscillators. oscillators coupled in a ring topology can generate multiphase outputs. For their nature, these oscillators operate off-resonance and consequently their phase noise worsens at increasing coupling strength. Since the coupling transistors raise the total power consumption, the noise-power product degrades even more with respect to a stand-alone oscillator. On the other hand, at high coupling factors, component mismatches affect less the phase accuracy. Closed-form expressions for phase noise and phase accuracy are derived which are verified against circuit simulations.

Design and Analysis on Bidirectionally and Passively Coupled QVCO With Nonlinear Coupler Nai-Chung Kuo, Jun-Chau Chien, and Ali M. Niknejad ,0018-9480 2015 IEEE. This paper studies quadrature voltage-controlled oscillators (QVCOs) employing bidirectional current injection from the two adjacent terminals and using a passive nonlinear coupler (BPN-QVCO). For such a QVCO to achieve quadrature locking while being robust to components mismatch, the odd-order nonlinearity of the coupling cell is essential and its significance in the performance merits is introduced. To verify the provided theory on BPN-QVCOs with resistive couplers, a modified diode is proposed as the coupling cell with doubled third-order nonlinearity for improved phase error without introducing additional capacitive loading. The proposed prototype and a standard 26-GHz BPNQVCO using conventional diode couplers are fabricated in 65-nm CMOS. The phase error due to the LC-tank mismatch is demonstrated to be half with the proposed coupling cell, verifying the theory. The proposed theory also applies to BPN-QVCOs using nonlinear capacitors as coupling cells.

The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking Ahmad Mirzaei, Mohammad E. Heidari, Rahim Bagheri, Saeed Chehrazi, and Asad A. Abidi, 0018-9200 2007 IEEE. We show that the quadrature LC oscillator is best treated as two strongly coupled, nominally identical oscillators that are locked to the same frequency. Differential equations that extend Adler's description of locking to strong injection reveal the full dynamics of this circuit. With a simplifying insight, the analysis reveals all the modes of the oscillator, their stability, the effects of mismatch on quadrature phase accuracy, and through a novel use of the analysis, phase noise.

Millimeter-Wave Beamforming as an Enabling Technology for 5G Cellular Communications: Theoretical Feasibility and Prototype ResultsWonil Roh, Ji-Yun Seol, JeongHo Park, Byunghwan Lee, Jaekon Lee, Yungsoo Kim, Jaeweon Cho, and Kyungwhoon Cheun. The ever growing traffic explosion in mobile communications has recently drawn increased attention to the large amount of underutilized spectrum in the millimeter-wave frequency bands as a potentially viable solution for achieving tens to hundreds of times more capacity compared to current 4G cellular networks. Historically, mmWave bands were ruled out for cellular usage mainly due to concerns regarding short-range and non-line-of-sight coverage issues. In this article, we present recent results from channel measurement campaigns and the development of advanced algorithms and a prototype, which clearly demonstrate that the mmWave band may indeed be a worthy candidate for next generation (5G) cellular systems. The results of channel measurements carried out in both the United States and Korea are summarized along with the actual free space propagation measurements in an anechoic chamber. Then a novel hybrid beamforming scheme and its link- and system-level simulation results are presented. Finally, recent results from our mmWave prototyping efforts along with indoor and outdoor test results are described to assert the feasibility of mmWave bands for cellular usage.

A Novel CMOS High-Power Terahertz VCO Based on Coupled Oscillators: Theory and Implementation Yahya M. Tousi, Omeed Momeni and Ehsan Afshari,0018-9200 2012 IEEE. We introduce a novel frequency tuning method for high-power terahertz sources in CMOS. In this technique, multiple core oscillators are coupled to generate, combine, and deliver their harmonic power to the output node without using varactors. By exploiting the theory of nonlinear dynamics, we control the coupling between the cores to set their phase shift and frequency. Using this method, two high-power terahertz VCOs are fabricated in a 65 nm LP bulk CMOS process. The first one has a measured output power of 0.76 mW at 290 GHz with 4.5% tuning range and the output power of the second VCO is 0.46 mW at 320 GHz with 2.6% tuning range. The output power of these signal sources is 4 orders of magnitude higher than previous CMOS VCOs and is even higher than VCOs implemented in compound semiconductors with much higher cut-off frequencies.

Performance of Coupled-Oscillator Arrays With Angle-Modulated Injection Signals Ana Collado and Apostolos Georgiadis 1549-8328 2010 IEEE. A nonlinear analysis of coupled-oscillator systems under modulated inputs is presented. Angle modulation is introduced to the array by injection locking one of the oscillators to an external modulated reference signal. Envelope transient analysis is used to investigate the effect of the modulation versus scanning angle. Furthermore, a simplified model for the array is provided based on a perturbation of the single-oscillator free-running steady state. In addition, arrays transmitting at the second

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harmonic are also examined, allowing for extended scanning range. Results are verified by measuring the performance of a fabricated two-element array operating at 4.5 GHz.

III.SIMULATION RESULTS

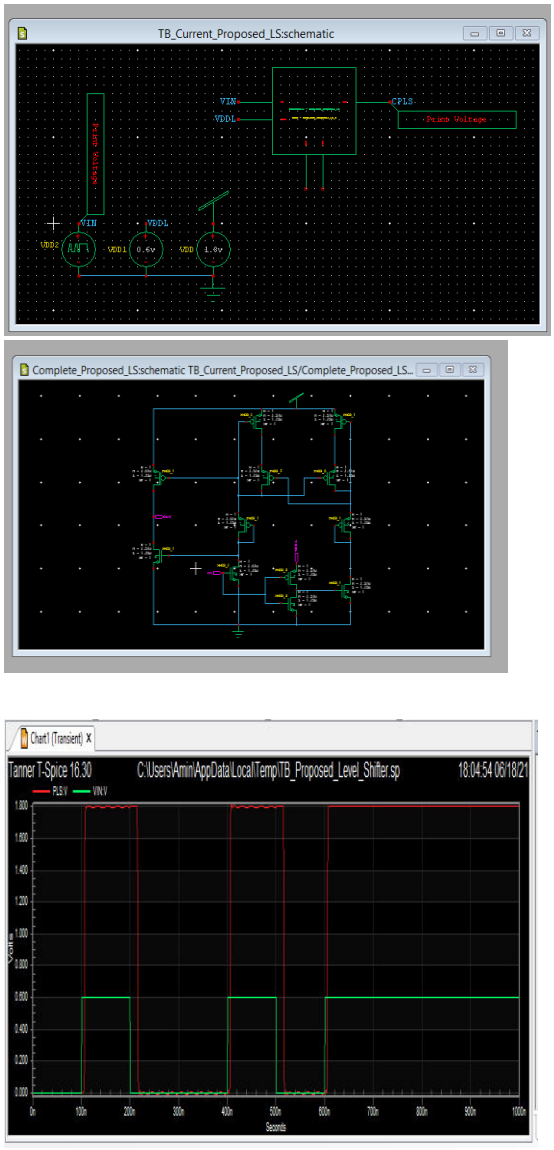

Fig.4 (a) Schematic of Proposed Level Shifter (b) Simulated Waveform

The Proposed Level Shifter is simulated in different technologies, 180nm, 45nm in Tanner EDA simulator in order to verify the performance in different technologies. Different types of level Shifters are also simulated keeping all the circuit parameters same as the parameters of the proposed circuit to have a fair comparison. Delay, power consumption and area of the circuits are compared

IV. COMPARISON

The circuits given here have been simulated in 45nm technology with input signal of 0.4/1.8 V and input frequency of 1 MHz are 123.1 nW and 23.7 ns, respectively.. The obtained voltage shifting level, power dissipation and delay are tabulated for comparison and given in table 1.1. The comparison table also mention the major drawback in each level shifter design.

table 1 Comparisons of Low Power and High Speed Voltage Level Shifter

	Comparisons of Low Power and High Speed Voltage Level Shifter at VDDH = 1.8V and VDDL = 0.6V							
	Current Mirror (CM)		Differential cascade voltage switch (DCVS)		Proposed level shifter (PLS)		Current Proposed level shifter (CPLS)	
	45nm	180nm	45nm	180nm	45nm	180nm	45nm	180nm
MOSFETs	8	8	8	8	10	10	12	12
Area (nm)	360	1440	360	1440	450	1800	540	2160
Power Consumed (mW)	14.94	128.0	70.85	373.5	2.814	3.0688	1.173	1.304
Delay (ns)	131.72	140.75	303.21	399.96	70.190	43.604	54.358	99.363

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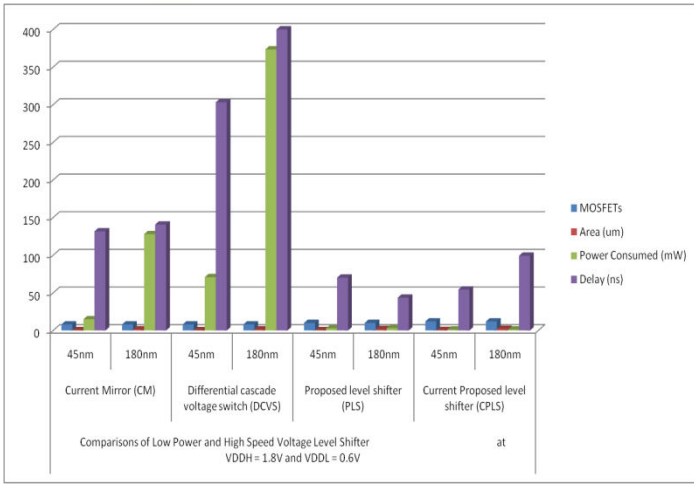

Fig.5 Comparison table of All model

V CONCLUSION

The efficient and very low power voltage level shifter is briefly discussed in the paper, the switching speed is increased day by day in analog and digital signal processing applications while the dynamic power consumption also decreased by adopting a new regulated cross coupled method of pull up network. The proposed level shifter may transform input signal with voltage levels far lower than a MOS device threshold voltage to greater nominal supply voltage levels. Even though to low number of components, the proposed level shifter method occupies a tiny silicon area with ultra low power consumptions by making it appropriate low power applications such as implanted medical devices and wireless sensor networks. the results of this work analyzed in Tanner EDA tool at 180 nm and 45 nm CMOS technology. The power dissipation and propagation delay of the proposed level shifter are 1.173 mW respectively, for low / high supply voltage of 0.4/1.8V and input frequency of 1 MHz .

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