International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Highly Efficient CNTFET-Based Unbalanced Ternary Logic Gates

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This study explores the potential benefits of employing ternary logic, particularly utilizing carbon nanotube field-effect transistors (CNTFETs), to mitigate power/energy consumption and area overhead in binary logic-based circuits. The paper focuses on designing and implementing highly efficient ternary logic gates including the standard ternary inverter (STI), ternary buffer (TBUF), ternary OR (TOR), and ternary AND (TAND) using CNTFET devices. Through simulations conducted with HSPICE software and the Stanford 32 nm CNTFET model at a 0.9 V supply voltage, the proposed designs demonstrate notable improvements in energy consumption and noise margin. Specifically, the proposed STI design showcases energy consumption reductions ranging from 12% to 91.17%, along with enhanced noise margin by at least 1.02×. The TBUF design exhibits energy consumption reductions between 14.73% and 96.82%. Moreover, the TOR design significantly reduces power dissipation and energy consumption by at least 73.82% and 86.70%, respectively, while the TAND design shows improvements of at least 9.58% and 12.48%, respectively.

The conventional binary logic system, relying on just two logical states, "0" and "1," necessitates numerous interconnections in very large-scale integrated (VLSI) circuits. These interconnectionsconstitute a significant portion of total power/energy consumption in VLSI circuits, leading to increased complexity and occupied space. Toaddress this, digital designers are turning to multiple-valued logic (MVL) systems, which offer at least three logical states, thus reducing interconnections and associated power/energy consumption. Thechoice of a base for computations is crucial for achieving highly energy-efficient systems. While the mathematical ideal is the irrationalconstant "e" (approximately 2.718), practical hardware constraints necessitate operations based on an integer. Previous research has demonstrated that the base "3," closest to "e" in complexity and cost,is optimal. The ternary logic system, based on three logical states "0," "1," and "2," presents an opportunity to reduce power dissipation and complexity. However, traditional ternary logic gates, such as ternary OR (TOR) and ternary AND (TAND), introduce challenges like increased power dissipation due to voltage division mechanisms.

This paper proposes highly efficient designs for ternary logic gates, leveraging carbon nanotube field-effect transistors (CNTFETs) to address these challenges. Specifically, CNTFET-based designs for ternary buffer (TBUF) and standard ternary inverter (STI) are introduced, enabling direct access to logic "1" from the power supply voltage VDD/2, thus minimizing power dissipation. Furthermore, efficient implementations of TOR and TAND gates are presented, reducing transistor count, delay, and overall power/energy consumption. In summary, the proposed designs leverage CNTFET technology to enhance the efficiency of ternary logic gates, offering significant reductions in power/energy consumption and complexity compared to traditional binary logic systems.

Based on the provided information, it seems that researchers are exploring the potential of implementing ternary logic circuits using carbon nanotube field-effect transistors (CNTFETs). These CNTFETs offer advantages over traditional silicon-based MOSFETs, especially as technology advances beyond the 32nm node. The ability of CNTFETs to exhibit different threshold voltages (Vth) based on the diameter of the carbon nanotubes enables the realization of ternary logic circuits. In ternary logic systems, three logical states, representedas "0", "1", and "2", are utilized. These states correspond to voltage levels of 0V, VDD/2, and VDD (where VDD is the operating supply voltage), respectively. Ternary logic gates such as ternary OR (TOR) and ternary AND (TAND) are crucial building blocks for designing ternary circuits. However, it's noted that the design and implementation of ternary NOR (TNOR) and ternary NAND (TNAND) gates are less common in current research efforts. To achieve TOR and TAND functionality, researchers often employ a standard ternary inverter (STI). This approach involves additional complexity, increasing transistor count, delay, and power/energy consumption. Therefore, there's an ongoing effort to optimize the design of ternary logic gates using CNTFETs to minimize these drawbacks. Overall, the use of CNTFETs in ternary logic circuits holds promise for overcoming challenges associated with traditional silicon-based technologies, and further research is focused on improving efficiency and reducing complexity in ternary gate implementations.

diode-connection are inserted into the designs to make a voltage division in the output to get logic "1", which increase the power dissipation. In this regard, we present highly-efficient TOR and TAND logic gates using CNTFET devices. Moreover, CNTFET- based ternary buffer (TBUF) and STI with low-energy consumption are proposed. In these designs, logic "1" is gotten directly from the power supply voltage $V_{DD}/2$ to remove the connection between V_{DD} and ground rails to reduce power dissipation.

Terminologies

It utilizes single-wall CNTs between the drain and the source contacts as a conducting channel.19 The CNT can be either metal or semiconductor relying on the integer pairs (n, m), known as chirality vector, which is the arrangement angle of carbon atom along the tube.7 If n is equal to m or their difference is a multiple of three, the CNT acts as a metal, and otherwise, it acts as a semiconductor.5 The relation between the CNT diameter (DCNT). X = ⌈2, 0, X = ′0′ [1a] else logic gates, respectively.19 Most recently published works7,8,11–13,20 have proposed TNOR and TNAND logic gates, where a standard ternary inverter (STI) is required to achieve TOR and TAND logic gates, respectively. This, in turn, increases the transistors count, delay, and power/energy consumption. Usually, ⌊two transistors with E-mail: murthujavali78618@gmail.com X = ⌊⌈0, X = ′2′ [1b] Proposed Designs This section proposes highly-efficient designs for the STI, TBUF, TOR, and TAND based on dual-VDD using CNTFET devices. The ternary logic system has twenty-seven logic gates with only one input and one output, known as unary operators.1 There are three types of inverters in the ternary logics are respectively.

$$XN = \begin{cases} 1, & x='0' \\ 0, & \text{else} \end{cases} \qquad [1a]$$

$$Xp = \begin{cases} 0, & X='1' \\ 1, & \text{else} \end{cases} \qquad [1b]$$

Proposed designs

The Proposed designs of the negative ternary inverters(NTI) and positive ternary inverters(PTI) are shown in below. We can define the designs are denoted in NTI is Xn and PTI is Xp

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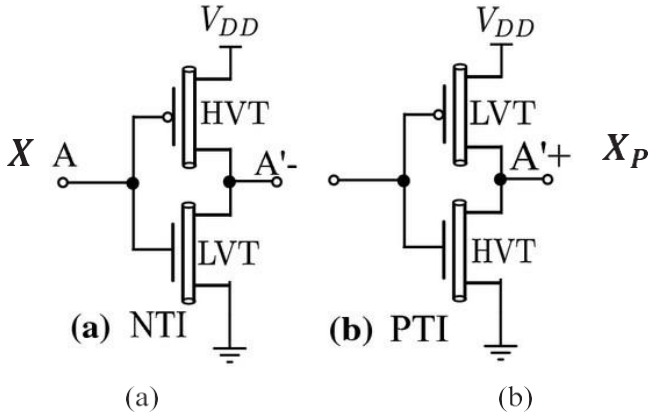

Figure 1. (a) NTI and (b) PTI.

Proposed standard ternary inverter.—An STI is a one-input one-output logic gate, where the output is the complement of the input. The STI can be expressed as Eq. 2, where X is the ternary input and X^- is the ternary output. The truth table of the STI is given in Table I. The structure of the proposed STI is shown in Fig. 2. When X = 0 V, transistor MP1 is turned on and charges X^- to V_{DD}. With an increase in the input voltage and reaching $V_{DD}/2$, X_1 is discharged to ground and turns on transistor MP4. Therefore, transistor MP4 charges X^- to $V_{DD}/2$. Finally, when X becomes V_{DD}, transistor MN1 is turned on and discharges X^- to ground.

$$X^- = 2 - X \quad [2]$$

Proposed ternary buffer.—A TBUF is a one-input one-output logic gate, where the output *TBUF* is equal to the input X. The truth table of the TBUF is given in Table II. The structure of the proposed TBUF is shown in Fig. 3. When the input X = 1 V, transistor MN1 is turned on and discharges the output *TBUF* to ground. With an increase in the input voltage and reaching $V_{DD}/2$, $\overline{X_1}$ is discharged to ground and turns on transistor MP4. Therefore, transistor MP4 charges *TBUF* to $V_{DD}/2$. Finally, when X becomes V_{DD}, transistor MP1 is turned on and charges *TBUF* to V_{DD}.

Proposed ternary OR logic gate.—A TOR logic gate is a two-inputs one-output logic gate, where the output *TOR* is the maximum of the given inputs X and Y, as given by Eq. 3. The truth table of the TOR logic gate is given in Table III. It is evident from this table that the output *TOR* can be easily implemented by satisfying the conditions mentioned below:

1) If X = "0" (X_N = "2"), then *TOR* = Y. This is implemented by a transmission gate formed by transistors MN1 and MP1, as depicted in Fig. 4.
2) If X = "1" ($\overline{X_1}$ = "0") and Y = "0" or "1", then *TOR* = "1", and if X = "2" (X_1 = "0") and Y = "2" (Y_P = "0"), then *TOR* = "2".

Table I. STI truth table.

Inputs	Unary operators			Output
X	X_N	X_P	$\overline{X_1}$	X^-
0	2	2	2	2
1	0	2	0	1
2	0	0	2	0

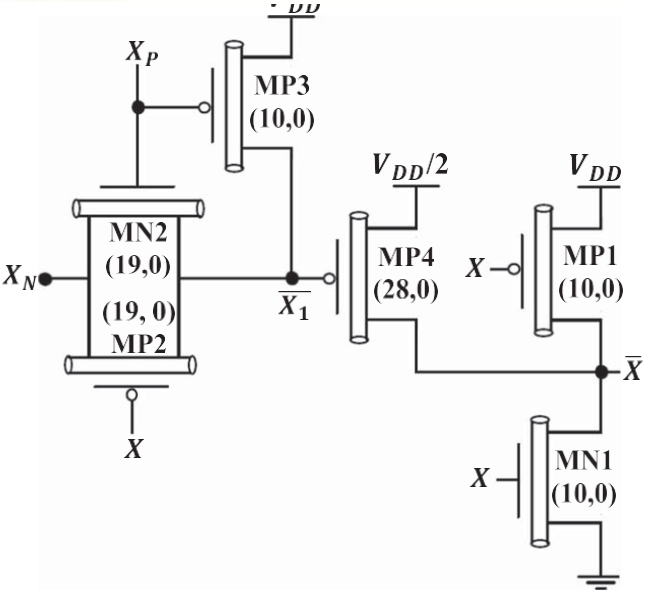

Figure 2. Proposed STI.

Table II. TBUF truth table.

Inputs	Unary operators			Output
X	X_N	X_P	$\overline{X_1}$	*TBUF*
0	2	2	2	0
1	0	2	0	1
2	0	0	2	2

This is implemented by transistors MN3 and MP2 to MP5, as depicted in Fig. 4.
3) If X = "1" (X_P = "1"), then *TOR* = "1". This is implemented by transistor MP7, as depicted in Fig. 4.

Figure 4 shows the complete structure of the proposed TOR logic gates. It can be implemented by using 16 CNTFET devices.

$$TOR = \max(Y, X) \quad [3]$$

Proposed ternary AND logic gate.—A TAND logic gate is a two-inputs one-output logic gate, where the output *TAND* is the minimum of the given inputs X and Y, as given by Eq. 4. The truth table of the TAND logic gate is given in Table IV. It is obvious fromthis table that the output *TAND* can be easily implemented by satisfying the following conditions:

1) If X = "0" (X_N = ""), Y = "0" (Y_N = "2"), or X = Y = "0" (X_N = X_N = "2"), then *TOR* = "0". This is implemented by transistors MN1 and MN2, as depicted in Fig. 5.
2) If X = "1" ($\overline{X_1}$ = "0") and Y = "1" or "2" (Y_N = "0"), then *TOR* = "1". This is implemented by transistors MN3 and MP1to MP4, as depicted in Fig. 5.
3) If X = "2" (X_P = "0"), then *TOR* = Y. This is implemented by transistor MP5, as depicted in Fig. 5.

The complete structure of the proposed TAND logic gate is shown in Fig. 5. It can be implemented by using 14 CNTFET devices.

$$TAND = \min(X, Y) \quad [4]$$

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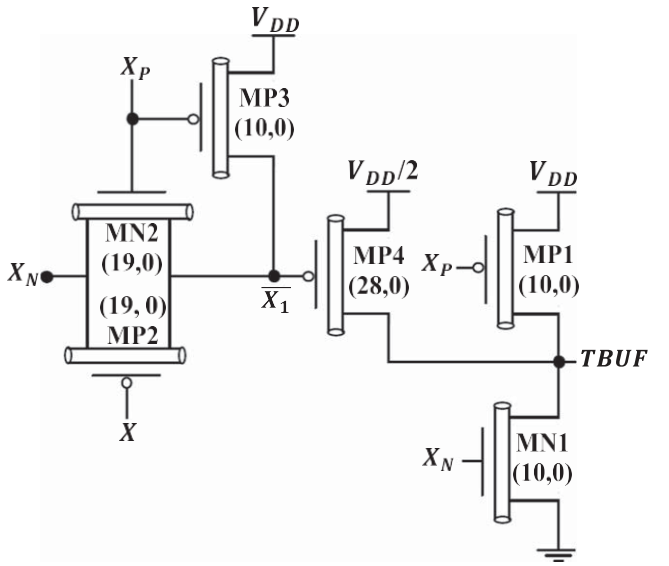

Figure 3. Proposed TBUF.

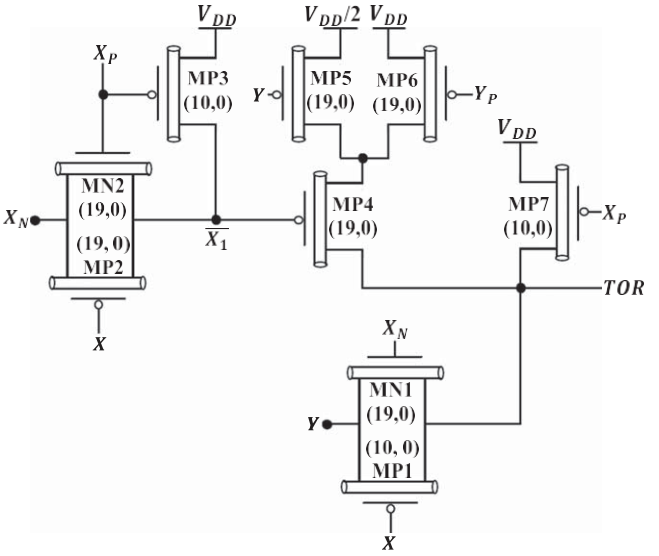

Figure 4. Proposed TOR.

Table III. TOR logic gate's truth table.

Inputs		Unary operators					
X	Y	X_N	X_P	$\overline{X_1}$	Y_N	Y_P	Output *TOR*
0	0	2	2	2	2	2	0
0	1	2	2	2	0	2	1
0	2	2	2	2	0	0	2
1	0	0	2	0	2	2	1
1	1	0	2	0	0	2	1
1	2	0	2	0	0	0	2
2	0	0	0	2	2	2	2
2	1	0	0	2	0	2	2
2	2	0	0	2	0	0	2

Table IV. TAND logic gate's truth table.

Inputs		Unary operators					
X	Y	X_N	X_P	$\overline{X_1}$	Y_N	Y_P	Output *TAND*
0	0	2	2	2	2	2	0
0	1	2	2	2	0	2	0
0	2	2	2	2	0	0	0
1	0	0	2	0	2	2	0
1	1	0	2	0	0	2	1
1	2	0	2	0	0	0	1
2	0	0	0	2	2	2	0
2	1	0	0	2	0	2	1
2	2	0	0	2	0	0	2

Performance Analyses and Discussions

The Stanford CNTFET model developed in Refs. 21, 22 and available in Ref. 23 with 32 nm physical channel length is used to simulate the proposed designs in the HSPICE software environment. The various performance metrics of the proposed designs including worst-case delay, average power consumption, and PDP are measured and compared with those of the designs presented in.[5,7,8,11,13,19,20,24,25] In these compared designs, the chirality vectors have been considered to be the same as specified in their original works, to have fair comparisons. Table V gives the CNTFET parameters used for simulations. Moreover, inputs have fall andrise times equal to 10 ps, output node is connected to 0.5 fF capacitive load, and frequency is set to 2 GHz.

Proposed STI performance. Figure 6 shows the inputs and outputs waveforms of the proposed STI. It can be seen from this figure that the proposed STI works well. The transient simulation results of the investigated STI designs have been summarized in Table VI. The proposed STI design uses 1.67×, 1.25×, 2×, and 2.5× higher number of transistors compared to the designs of Refs. 5, 7, 8, 11, 13, and[20] respectively, and has 28.57% lower number of transistors than that of the design of Ref. 25. However, it reduces the delay by 27.68%, 22.67%, 15.70%, 5.54%, and 16.18% in comparison with the designs of Refs. 5, 7, 8, 11, 13 and 25 respectively, and incurs a penalty of 1.08× in the delay compared to the design of Ref. 20. Moreover, it shows improvements of 78.02%, 89.53%, 77.19%, 45.83%, 85.32%, and 74.58% in the power consumption compared to the designs of Refs. 7, 8, 11, 13, 20, and 25 correspondingly, and incurs a penalty of 1.14× in this performance metric in contrast with the design of Ref. 5. The PDP of the proposed STI design is the lowest, which is improved by 80.86%, 12%, 91.17%, 80.77%, 48.84%, 84.17%, and 78.69 as compared to the designs of Refs. 5, 7, 8, 11, 13, 20 and 25 respectively.

Figure 7 shows the overlapped voltage transfer characteristics (VTCs) of the proposed STI design to measure the noise margin (NM). The NM value depends on the side length of the largest square drawn within the smaller wing.[19] The overlapped VTCs of the proposed STI design show four NMs such as NM_H, NM_{MH},NM_{ML}, and NM_L. Owing to being symmetry, $NM_H = NM_L$ and $NM_{MH} = NM_{ML}$. The maximum of these four NMs is considered as NM. The DC simulation results of the studied STI designs have beengiven in Table VII. The proposed STI design shows the highest NM,improving it by 1.67×, 1.08×, 2.5×, 1.25×, 3.75×, 1.15×, and 1×
as compared to the designs of Refs. 5, 7, 8, 11, 13, 20 and 25 respectively.

Proposed TBUF performance. Figure 8 shows the inputs and outputs waveforms of the proposed TBUF design, which imply the correct operation of the proposed TBUF design. Table VIII compares the various performance metrics such as the transistors count, delay, power consumption, and PDP of the investigated TBUF designs. The proposed TBUF design increases the transistors count by 1.67× and 1.25× compared to the designs of Refs. 7 and 5

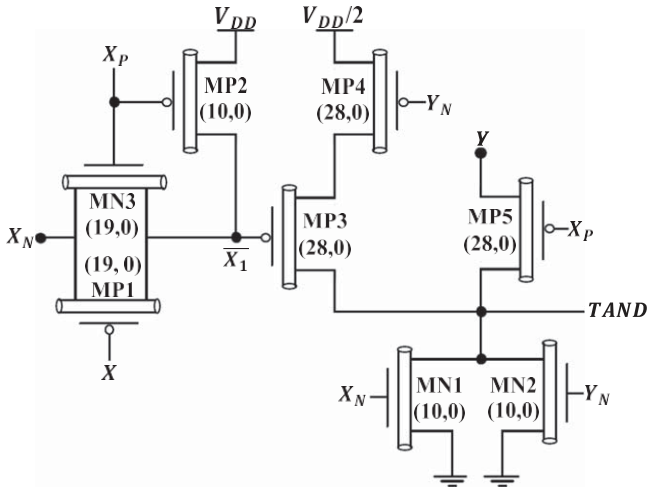

Figure 5. Proposed TAND.

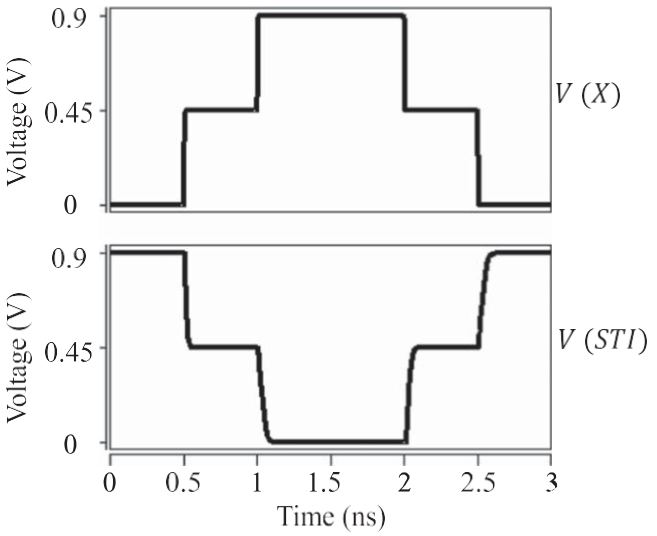

Figure 6. Transient response of the proposed STI at V_{DD} = 0.9 and 27 °C.

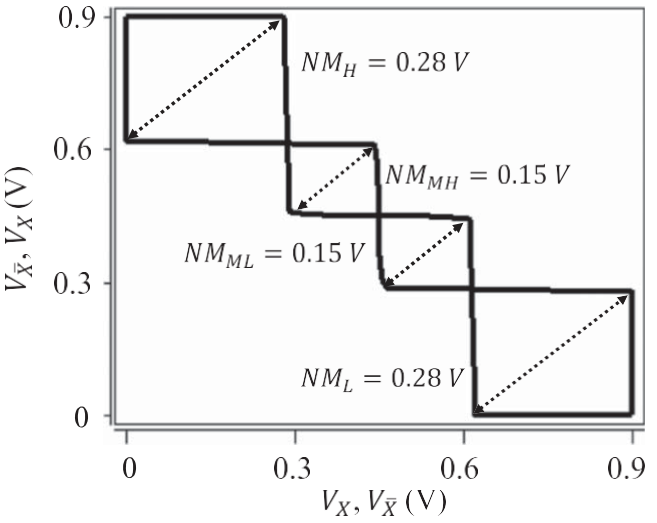

Figure 7. The overlapped VTCs of the proposed STI, along with NM values, at V_{DD} = 0.9 and 27 °C.

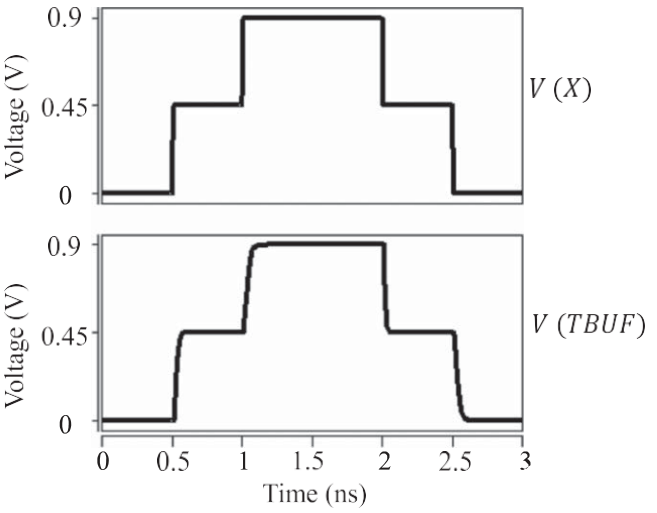

Figure 8. Transient response of the proposed TBUF at V_{DD} = 0.9 and 27 ° C.

respectively, uses the same number of transistors as those of the designs of Refs. 19, 24, and reduces it by 29.57% compared to the design of Ref. 25. The delay in the proposed TBUF design increases by 3.53× and 2.05×, and improves by 25.39%, 7.87%, and 61.73% in comparison with the designs of Refs. 5, 7, 19, 24 and 25 respectively. Moreover, the proposed TBUF design consumes a 2.11× higher power than that of the design presented in Ref. 5 and

Table V. CNTFET parameters used for simulations.

Parameter	Value
Physical channel length	30 nm
The mean free path in the intrinsic CNT	202 nm
The length of the doped CNT drain-side region	17 nm
The length of the doped CNT source-side region	18 nm
The mean free path in the p+/n+ doped CNT	19 nm
The Fermi level of the doped S/D CNT	0.56 eV
The dielectric constant of high-k top gate dielectric material (HfO_2)	17
The dielectric constant of the substrate (SiO_2)	3
The thickness of the high-k top gate dielectric material	3 nm
The coupling capacitance between the channel region and the substrate (SiO_2)	20 aF μm^{-1}
The coupling capacitance between the channel region and the source/drain islands	0 aF/μm
The distance between two adjacent CNTs within the same device	30 nm
The work function of the S/D metal contacts and CNT	3.5 eV
The number of tubes in the device	1

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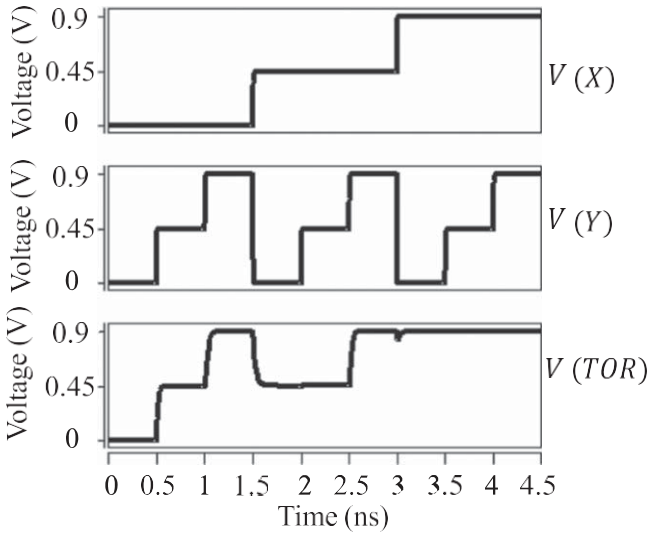

Figure 9. Transient response of the proposed TOR logic gate at V_{DD} = 0.9 and 28 °C.

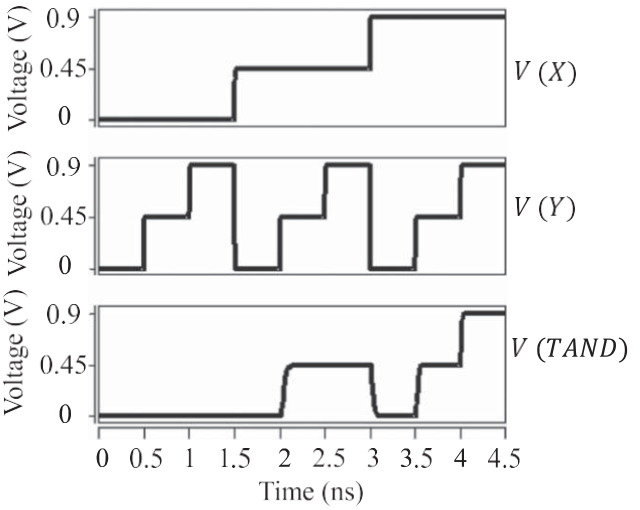

Figure 10. Transient response of the proposed TAND logic gate at V_{DD} = 0.9 and 28 °C.

offers at least 78.76% improvement in the power consumption compared to the rest designs. Furthermore, the PDP in the proposed TBUF design is improved by at least 15.73%.

Proposed TOR performance. To ensure that the proposed TOR design works correctly, its inputs and outputs waveforms are shown in Fig. 9. From Table IX, which gives a performance comparison of the examined TOR designs, it is concluded that the proposed TOR design offers 1.07× and 1.5× higher transistors number than those of the designs of Refs. 19 and 20 and reduces it by 7.25% and 2.67% compared to the designs of Refs. 7, 8, 11 and 25 respectively. The proposed TOR design improves the delay/power/ PDP by 42.44%/72.62%/84.80%, 45.10%/75.22%/85.91%, 41.25%/ 76.71%/86.33%,51.65%/80.50%/89.61%, and 21.14%/84.62%/ 88.87% when compared with the designs of Refs. 7, 8, 11, 19 and 20 respectively. When the proposed TOR design is compared with the design of Ref. 25, the delay is increased by 1.29× and the power and PDP are reduced by 98.05% and 96.18%, respectively.

Proposed TAND performance. The inputs and outputs waveforms of the proposed TAND logic gate are shown in Fig. 10, which can be seen that it works well. A performance comparison between the proposed and the other existing TAND designs has been performed in Table X. The proposed TAND design reduces the number of transistors by 12.50%, 6.67%, 22.22% compared to the designs of Refs. 6, 7, 12, 13 and 25 respectively, and increases it by 1.4× compared to the designs of Ref. 20. It also improves the delay by 22.50%, 9.57%, 5.81%, 25.27%, and 5.04%, reduces the power consumption by 73.84%, 76.43%, 79.89%, 77.50%, and 9.55%, and decreases the PDP by 80.20%, 79.22%, 76.52%, 83.48%, and 12.38% compared to the designs presented in Refs. 7, 8, 11, 19 and 13, respectively. Moreover, when the proposed TAND design is compared with the designs of Refs. 20 and 25, the delay is increased by 1.30× and 2.06×, the power consumption is improved by 90.36%

Table VI. Simulation outcomes of the proposed STI and the other STI circuits available in the literature (V_{DD} = 0.9 V, 24°C, 0.2 fF capacitive load).

STI circuit	Transistors count	Worst-case delay (ps)	Average power (μW)	PDP (aJ)
In Ref. 7	6	34.4	0.869	29.89
In Ref. 20	4	26.9	0.620	16.68
In Ref. 11	6	40.1	0.414	13.79
In Ref. 8	6	34.4	0.399	13.73
In Ref. 25	14	34.6	0.358	12.39
In Ref. 13	5	30.7	0.168	5.16
In Ref. 5	8	37.5	0.08	3
Proposed	10	29	0.091	2.64

Table VII. Noise margins results of the proposed STI and the other STI circuits available in the literature (V_{DD} = 0.9 V, 25 °C).

STI circuit	NM_H (V)	NM_{MH} (V)	NM_{ML} (V)	NM_L (V)	NM (V)
In Ref. 13	0.27	0.04	0.04	0.27	0.04
In Ref. 7	0.24	0.06	0.06	0.24	0.06
In Ref. 11	0.24	0.09	0.09	0.24	0.09
In Ref. 8	0.24	0.12	0.12	0.24	0.12
In Ref. 20	0.13	0.13	0.14	0.13	0.13
In Ref. 5	0.28	0.14	0.14	0.28	0.14
In Ref. 25	0.24	0.15	0.15	0.24	0.15
Proposed	0.28	0.15	0.15	0.28	0.15

Table VIII. Simulation outcomes of the proposed TBUF and the other TBUF circuits available in the literature (V_{DD} = 0.9 V, 27 °C, 0.6 fF capacitive load).

TBUF circuit	Transistors count	Worst-case delay (ps)	Average power (μW)	PDP (aJ)
In Ref. 7	8	10.8	8.24	88.43
In Ref. 25	13	64	1.073	76.92
In Ref. 24	14	42	0.468	18.02
In Ref. 19	14	25.3	0.451	10.63
In Ref. 5	9	36.9	0.042	4.19
Proposed	11	27.8	0.051	3.72

Table IX. Simulation outcomes of the proposed TOR and the other TOR circuits available in the literature (V_{DD} = 0.9 V, 29 °C, 0.3 fF capacitive load).

TOR circuit	Transistors count	Worst-case delay (ps)	Average power (μW)	PDP (aJ)
In Ref. 24 (TOR)	15	15.18	2.793	78.88
In Ref. 10 (TNOR+STI)	16	53.8	0.536	55.32
In Ref. 16 (TNOR+STI)	13	28.6	0.724	41.69
In Ref. 4 (TNOR+STI)	18	43	0.478	49.24
In Ref. 3 (TNOR+STI)	19	42.8	0.487	38.67
In Ref. 19 (TOR)	11	40.6	0.409	57.30
Proposed TOR	10	26.8	0.145	3.63

Table X. Simulation outcomes of the proposed TAND and the other TAND circuits available in the literature (V_{DD} = 0.9 V, 28°C, 0.4 fF capacitive load).

TAND circuit	Transistors count	Worst-case delay (ps)	Average power (μW)	PDP (aJ)
In Ref. 23 (TAND)	18	20	4.786	78.74
In Ref. 19 (TNAND+STI)	10	31.5	0.765	29.95
In Ref. 18 (TNAND+STI)	16	54.8	0.547	54.61
In Ref. 17 (TAND)	14	52.2	0.464	46.35
In Ref. 7 (TNAND+STI)	16	42.7	0.409	19.67
In Ref. 6 (TNAND+STI)	16	44.9	0.423	21.39
In Ref. 12 (TNAND+STI)	15	42.8	0.145	4.01
Proposed TAND	14	41.5	0.176	5.44

and 98.17%, and the PDP is reduced by 83.66% and 93.14%, respectively.

Conclusions

Carbon nanotube field-effect transistors (CNTFETs) are emerging as promising candidates to replace Silicon-based metal-oxide-semiconductor field-effect transistors (Si-MOSFETs) beyond the 32 nm technology node due to their ability to mitigate scaling difficulties and offer high performance. Meanwhile, the utilization of multiple- valued logic (MVL) presents a solution to the limitations of binary logic in designing very large-scale integrated (VLSI) circuits, addressing issues such as increased interconnections, complexity, area overhead, response time, and power consumption. In CNTFET devices, the threshold voltage can be controlled by adjusting the carbon nanotube diameter, making them suitable for implementing ternary VLSI circuits.In this study, efficient designs for ternary logic gates, including the standard ternary inverter (STI), ternary buffer(TBUF), ternary OR (TOR), and ternary AND (TAND), were proposed and implemented using CNTFET devices. Various performance metrics of the proposed designs were evaluated using HSPICE software with the Stanford 34 nm CNTFET model at a 0.9 V supply voltage. The results indicate significant improvements in energy consumption, with the proposed STI and TBUF designs showing enhancements ranging from 14% to 89.27% and from 16.83% to 97.82%, respectively.consumption, respectively. Moreover, the proposed TOR design reduced power dissipation and energy consumption by at least 74.62% and 83.80%, while the proposed TAND design improved them by at least 8.55% and 11.38%, respectively.

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