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BIST to Test Low-Power Pseudorandom Pattern Generators

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Abstract:- *This project describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in self-test (BIST)- based pseudorandom test pattern generators. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage-to pattern-count ratios. Furthermore, this proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO based logic BIST (LBIST) infrastructure. The proposed architecture is extended in such that the patterns generated from PRPG is gone through CUT and then to TRA to perform ATE.* ***Keywords:*** *Test Data Volume Compression, Built-In Self-Test (BIST), Low-Power (LP) Test, Pseudorandom Test Pattern Generators (PRPGS)*

1. INTRODUCTION

Power Dissipation is a conundrum in modern System-on-Chips Design and Testing. In VLSI circuits, built in self- test (BIST) are utilized for testing. The function of the BIST is to reduce power dissipation without affecting to the fault coverage .The main challenging areas in VLSI are performance, cost, testing, area, reliability and puissance. The authoritative ordinance for portable computing contrivances, daily life equipment's, and communication system are incrementing rapidly. Built-in self-test is a design technique where components of a circuit are acclimated to test the circuit itself. Built in self-test is the capability of the circuit to test itself. BIST represents converge of concept of built in test and self -test and hence come to be synonymous with these terms. The potency dissipation during test mode is 200% more than in mundane mode. Hence the paramount aspect to optimize power during testing. Four reasons are responsible for power increase during test. High switching activity due to test patterns Parallel activation of internal cores during test Power consumed by extra DFT circuitry Low correlation among test vectors Main purport of testing is to detect malfunctions in the hardware of product and to locate their reason so that they may be eliminated. In others words the aim of testability is

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to do the components testable not only on test fixtures particular from the system but withal within the system when the components are connected. Design for test, DFT must be a central element of any design process these days. With circuit promiscuity protrude and component size decrementing, the testability of electronic circuits is more deciding as testing is becoming ever more injuctively authorizing. The only way that tolerable testing can be obtain by employing design for test. DFT is a technique, which facilitates a design to become testable after engenderment. Its the extra plausible which we inserted the simple design, during the design process, which avails its post-engenderment testing afore engenderment testing is must because, the process of engenderment is not 100% error free. There are fault in silicon which contribute to the fault in the contrivance.

2. RELATED WORK

Subsisting System

An n-bit PRPG connected with a phase shifter alimenting scan chains forms a kernel of the engenderer engendering the authentic pseudorandom test patterns. A linear feedback shift register or a ring engenderer can implement a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is verbalized to be in the toggle mode. When the latch is incapacitated, it captures and preserves, for a number of clock cycles, the corresponding bit of PRPG, thus victualing the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches. Consequently, every scan chain remains in a low-power mode provided only incapacitated hold latches drive the corresponding phase shifter output the toggle control register supervises the hold latches Its content comprises 0s and 1s, where 1s denote latches in the toggle mode, thus transparent for data arriving from the PRPG. Their fraction determines a scan switching activity.

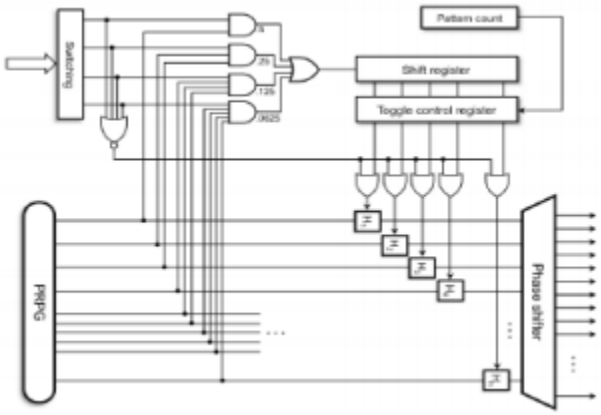

Fig:-1 Basic architecture of a PRESTO generator.

The control register is reloaded once per pattern with the content of an adscititious shift register. The enable signals injected into the shift register are engendered in a probabilistic fashion by utilizing

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the pristine PRPG with a programmable set of weights. The weights are resolute by four AND gates engendering 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate sanctions culling probabilities beyond simple powers of 2. A 4-bit register Switching is employed to activate AND gates, and sanctions culling a utilizer-defined level of switching activity. For example, the switching code 0100 will set to 1, on the average, 25% of the control register stages, and thus 25% of hold. Latches will be enabled. Given the phase shifter structure, one can assess then the amount of scan chains receiving constant values, and thus the expected toggling ratio. An adscititious 4-input NOR gate detects the switching code 0000, which is utilized to switch the LP functionality off. It is worth noting that when working in the weighted arbitrary mode, the switching level selector ascertains statistically stable content of the control register in terms of the amount of 1s it carries. As a result, roughly the same fraction of scan chains will stay in the LP mode, though a set of genuine low toggling chains will keep transmuting from one test pattern to another. It will correspond to a certain level of toggling in the scan chains. With only 15 different switching codes, however, the available toggling granularity may render this solution too coarse to be always acceptable. While preserving the operational principles of the rudimental solution, this approach splits up a shifting period of every test pattern into a sequence of alternating hold and toggle intervals.

Proposed System

In order to facilitate test data decompression while preserving its pristine functionality. The core principle of the decompressor is to incapacitate both weighted logic blocks (V and H) and to deploy deterministic control data instead. In particular, the content of the toggle control register can now be culled in a deterministic manner due to a multiplexer placed in front of the shift register. Furthermore, the Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and thus to determine durations of the hold and toggle phases. When this circuit reaches the value of zero, it causes a dedicated signal to go high in order to toggle the T flipflop. The same signal sanctions the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop need to be initialized every test pattern. The initial value of the T flipflop decides whether the de-compressor will commence to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, determines that mode's duration.

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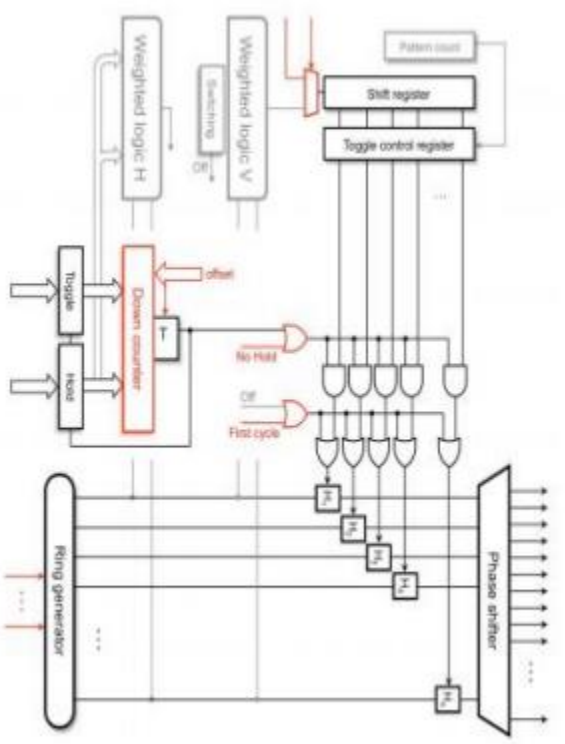

Fig:-2 LP Decompressor

As can be optically discerned, functionality of the T flip-flops remains identically tantamount to that of the LP PRPG but two cases. First of all, the encoding procedure may consummately incapacitate the hold phase (when all hold latches are blocked) by loading the Hold register with an opportune code, for example, 0000. If detected (No Hold signal in the figure), it overrides the output of the T flip-flop by utilizing a supplemental OR gate, as shown in Fig. 4. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In integration, all hold latches have to be opportunely initialized. Hence, control signal First cycle engendered at the cessation of the ring engenderer initialization phase reloads all latches with the current content of this component of the decompressor.

3. IMPLEMENTATION

ROM One method is to store a good test-pattern set (from an ATPG program) in a ROM on the chip.

LFSR Another method is to utilize a linear feedback shift register (LFSR) to engender pseudo-arbitrary tests.

Binary Counter A binary counter can engender an entire test sequence, but this can utilize very much test time if the number of inputs is prodigiously and sizably voluminous.

Modified Counters Modified counters have additionally been prosperous as test-pattern engenderers, but they withal go for long test sequences.

FSR and ROM For primary test mode, the most efficacious approaches is to utilize an LFSR to engender test-patterns with an ATPG program. These supplemental test-patterns can either be stored in a ROM on the chip for a second test, they can be applied in a scan chain in order to logic the stuck-fault coverage to 100%.

Cellular Automaton In this approach, each pattern engenderer cell has a logic gates, a flip-flop to connections only to neigh bouring gates. The cell is respond to engender the cellular automaton.

4. EXPERIMENTAL RESULTS

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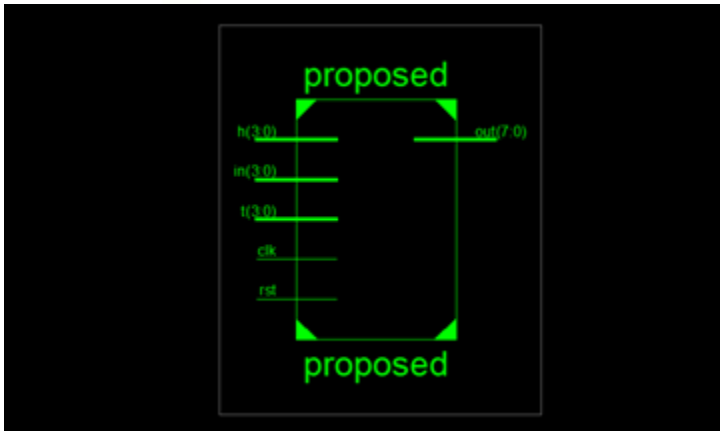

Fig:-3 Block diagram

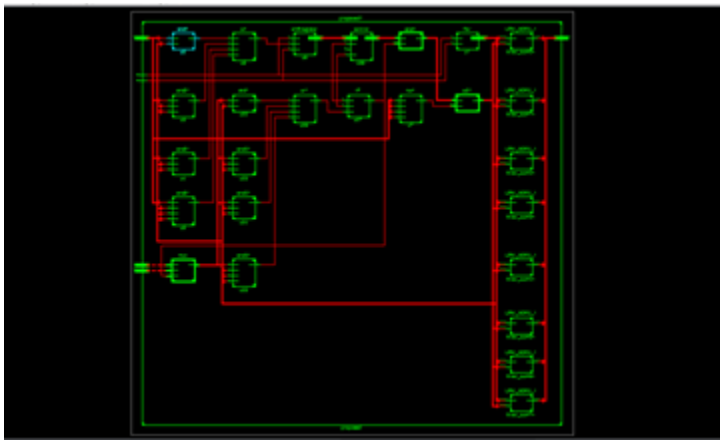

Fig:-4 Circuit

Fig:-5 Final Result

5. CONCLUSION

The incipiently proposed low power PRPG is capable of acting as a plenarily functional test data decompressor with competency to precisely control scan shift-in switching activity through the process of encoding, while its low power test logic requires considerably more minuscule amount of silicon authentic estate than that of the subsisting low power compression schemes. The proposed hybrid solution sanctions one to efficiently cumulate test compression with logic BIST, where both techniques can work synergistically to distribute high quality test. It is ergo a very alluring low power test scheme that sanctions for trading-off test coverage, pattern counts and toggling rates.

6. REFERENCES

[1] A. S. Abu-Issa and S. F. Quigley, “Bit swapping LFSR for low-power BIST,” Electron. Lett., vol. 44, no. 6, pp. 401–402, Mar. 2008.

[2] C. Barnhart et al., “Extending OPMISR beyond 10x scan test efficiency,” IEEE Design Test, vol. 19, no. 5, pp. 65–73, Sep./Oct. 2002.

[3] V.D. Agrawal and M. Bushnell, Essentials of Electronic Testing For Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.

[4] N.Ahmed, M. H. Tehranipour, M. Nourani, “Low Power Pattern Generation for BIST Architecture”, IEEE Circuits and Systems, 2004. ISCAS '04. Proceedings of the International

Symposium, 23-26 May 2004, Vol. 2, pages 689-92., 2004

[5] M. Bellos, D. Bakalis, D.Nikolos, X. Kavousianos, "Low Power Testing by vector Ordering with Vector Repetition", pp 205-210,2004.

[6] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, "A Gated Clock Scheme for Low Power Scan-Based BIST" Proceedings of the Seventh IEEE International On-Line Testing Workshop (IOLTW'01), 2001.

[7] Walter Aloisi and Rosario Mita, Member, IEEE, Gated clock design of Linear Feedback Shift Register , IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 55, NO. 6, JUNE 2008.

[8] Deterministic and Low Power BIST Based on Scan Slice Overlapping, Ji Li Yinhe Han Xiaowei Li, Proc.of NSFC, pp. 5670-5673, 2005.