International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

A NEW TOPOLOGY OF THREE PHASE SYMMETRICAL MULTILEVEL CONVERTER FOR GRID CONNECTED SYSTEM

[1]Mr.CH. PRATAPA REDDYM.Tech, [2]AKKALA. ANIL KUMAR REDDY, [3]ARIGELA. VEERA VENKATA SANTOSH, [4]LAGUDU VIJAYA BHARGAV, [5]PATNANA DIVAKAR, [6]CHINTHAMALLA MANOHAR KUMAR

[1]ASSISTANT PROFESSOR,[23456]B.Tech Students,

DEPARTMENT OF EEE, ABR COLLEGE OF ENGINEERING AND TECHNOLOGY

KANIGIRI(M), PRAKASAM DIST-523230(A.P)

ABSTRACT

Nowadays multilevel inverters are developing generally due to reduced voltage stress on power switches and low total harmonic distortion (THD) in output voltage. However, for increasing the output voltage levels the number of circuit devices are increased and it results in increasing the cost of converter. In this paper, a novel multilevel inverter is proposed. The suggested topology uses less number of power switches and related gate drive circuits to generate the same level in output voltage with comparison to traditional cascaded multilevel inverter. With the proposed topology all levels in output voltage can be realized. As an illustration, a symmetric 13-level and asymmetric 29-level proposed inverters have been simulated and implemented. The total peak inverse (PIV) and power losses of presented inverter are calculated and compared with conventional cascaded multilevel inverter. In this paper, a new structure for multilevel voltage source inverter is introduced, which produces more number of levels at output voltage waveform with reduced number of IGBTs and gate drivers. The number of required IGBTs and drivers against voltage levels is very important factors in designing of multilevel inverter, because IGBTs and drivers define the cost, reliability, circuit size, installation area and control complexity. For proposed multilevel inverter, three methods for determination of voltage sources values are presented. A comparison is presented between proposed structure and the classical multilevel inverter structures and another structure are presented to reflect the merits of the presented structure. The validity of the proposed multilevel inverter is verified with computer simulation and experimental results. Fundamental frequencyswitching method has been applied to the new topologies to trigger the power switches for controlling the voltage levels generated on the output.

Keywords:Multilevel converter, Grid-connected system, Voltage source inverter, Power switches, Total harmonic distortion, Gate drive circuits, Experimental validation

INTRODUCTION

Multilevel inverters have garnered significant attention in recent years owing to their ability to mitigate voltage stress on power switches and reduce total harmonic distortion (THD) in the output voltage [1]. These inverters are pivotal in numerous applications, particularly in grid-connected systems where maintaining high-quality power is paramount [2]. However, a common challenge associated with traditional multilevel inverters is the escalating number of circuit devices required to achieve higher output voltage levels [3]. This increase in circuit complexity inevitably leads to a rise in the overall cost of the converter, posing a barrier to widespread adoption [4].In response to this challenge, this paper proposes a novel multilevel inverter topology designed to address the limitations of conventional cascaded multilevel inverters [5]. The proposed topology offers a compelling alternative by employing fewer power switches and associated gate drive circuits while delivering comparable output voltage levels [6]. By leveraging innovative circuit configurations, the proposed topology enables the realization of all voltage levels in the

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

output waveform, thereby enhancing flexibility and performance [7]. To illustrate its effectiveness, symmetric 13-level and asymmetric 29-level inverters based on the proposed topology have been simulated and implemented [8].

A critical aspect of any inverter design is the assessment of its performance in terms of peak inverse voltage (PIV) and power losses [9]. In this regard, the total PIV and power losses of the presented inverter are meticulously calculated and compared against conventional cascaded multilevel inverters [10]. The results of these comparisons offer valuable insights into the efficacy and efficiency of the proposed topology, highlighting its potential to deliver superior performance while minimizing costs [11].Furthermore, the paper introduces a new structure for multilevel voltage source inverters that achieves a higher number of output voltage levels with a reduced number of insulated gate bipolar transistors (IGBTs) and gate drivers [12]. This optimization is crucial as the number of required IGBTs and gate drivers significantly impacts the overall cost, reliability, circuit size, installation area, and control complexity of the inverter system [13]. To facilitate the determination of voltage source values for the proposed multilevel inverter, three distinct methods are presented, offering designers a comprehensive toolkit for optimization [14].

To underscore the advantages of the proposed structure, a comparative analysis is conducted with classical multilevel inverter structures, showcasing the merits and superior performance of the presented topology [15]. Additionally, another structure is introduced to further emphasize the unique attributes of the proposed topology and its potential applications in various scenarios [16]. The validity and effectiveness of the proposed multilevel inverter are verified through rigorous computer simulations and experimental results [17].Fundamental frequency switching methods are employed in the new topologies to trigger the power switches, enabling precise control over the voltage levels generated on the output [18]. This approach ensures robust and reliable operation, further enhancing the appeal and applicability of the proposed multilevel inverter topology in grid-connected systems [19]. In summary, the introduction of this novel topology represents a significant advancement in the field of multilevel converters, offering a cost-effective solution with enhanced performance and flexibility for grid-connected applications.

LITERATURE SURVEY

The evolution of multilevel inverters represents a significant advancement in power electronics, driven by the quest for reduced voltage stress on power switches and minimal total harmonic distortion (THD) in output voltage. These inverters have gained prominence across various applications, particularly in grid-connected systems where high-quality power delivery is imperative. Traditional multilevel inverters have been successful in achieving these objectives to some extent. However, as the demand for higher output voltage levels escalates, the inherent challenge of increasing the number of circuit devices arises. This proliferation of circuit components inevitably leads to a rise in the overall cost of the converter, posing a significant barrier to widespread adoption.

In response to these challenges, researchers and engineers have been actively exploring novel approaches to multilevel inverter design. One such approach involves the development of innovative topologies that utilize fewer power switches and related gate drive circuits while delivering comparable output voltage levels. By optimizing circuit configurations and leveraging advanced control strategies, these new topologies aim to achieve all levels in the output voltage waveform, thereby enhancing flexibility and performance. This paradigm shift holds immense promise in addressing the cost and complexity issues associated with traditional multilevel inverters.As part of this literature survey, various studies have investigated the performance and feasibility of alternative multilevel inverter topologies. Researchers have conducted simulations and implemented prototype inverters to validate the effectiveness of these new designs. Notably, symmetric and asymmetric multilevel inverters with a wide range of output voltage levels have been studied extensively. These investigations have shed light on the potential benefits of utilizing novel topologies in practical applications, paving the way for further exploration and refinement.

A key aspect of multilevel inverter design is the assessment of peak inverse voltage (PIV) and power losses. Researchers have devoted considerable effort to analyzing and comparing these parameters between conventional cascaded multilevel inverters and proposed novel topologies. Through meticulous calculations and simulations, valuable insights have been gained into the efficiency and performance trade-offs associated with different inverter configurations. These findings are instrumental in guiding the selection and optimization of multilevel inverter designs for specific applications.Moreover, researchers have proposed new structures for multilevel voltage source inverters aimed at maximizing the number of output voltage levels while minimizing the number of insulated gate bipolar transistors (IGBTs) and gate drivers. This optimization is crucial as the number of required components directly impacts the cost, reliability, circuit size, installation area, and control complexity of the inverter system. By presenting multiple methods for determining voltage source values, researchers have empowered designers with the tools needed to optimize the performance and cost-effectiveness of multilevel inverters.

In addition to theoretical studies, comparative analyses have been conducted between proposed novel structures and classical multilevel inverter configurations. These comparisons highlight the strengths and weaknesses of different approaches, providing valuable insights into the relative merits of each design. By evaluating factors such as cost, reliability, circuit size, and control complexity, researchers aim to identify the most promising solutions for practical implementation.Overall, the literature survey underscores the dynamic nature of multilevel inverter research and development. Through a combination of theoretical analyses, simulations, and experimental validation, researchers continue to push the boundaries of innovation in pursuit of more efficient, cost-effective, and reliable multilevel converter technologies. The insights gained from these studies pave the way for advancements in grid-connected systems and other applications where high-quality power delivery is paramount.

PROPOSED SYSTEM

In recent years, multilevel inverters have garnered increasing attention within the field of power electronics due to their ability to alleviate voltage stress on power switches and minimize total harmonic distortion (THD) in the output voltage. These inverters play a pivotal role in various applications, particularly in grid-connected systems, where the delivery of high-quality power is paramount. However, a persistent challenge in the development of multilevel inverters is the escalation in the number of circuit devices required to achieve higher output voltage levels. This increase in circuit complexity inevitably leads to a rise in the overall cost of the converter, thus impeding widespread adoption across industries.In response to these challenges, this paper proposes a novel topology for a three-phase symmetrical multilevel converter designed to address the limitations of traditional cascaded multilevel inverters. The key innovation of the suggested topology lies in its ability to generate the same level of output voltage using fewer power switches and associated gate drive circuits compared to conventional cascaded multilevel inverters. This reduction in circuit complexity is achieved without compromising the ability to realize all levels in the output voltage waveform. To illustrate the effectiveness of the proposed topology, symmetric 13-level and asymmetric 29-level inverters have been simulated and implemented.

A critical aspect of evaluating the performance of multilevel inverters is the assessment of peak inverse voltage (PIV) and power losses. In this paper, the total PIV and power losses of the presented inverter are meticulously calculated and compared with those of conventional cascaded multilevel inverters. This comparative analysis provides valuable insights into the efficiency and effectiveness of the proposed topology, highlighting its potential to deliver superior performance while minimizing costs.Furthermore, this paper introduces a new structure for multilevel voltage source inverters aimed at maximizing the number of output voltage levels while reducing the number of insulated gate bipolar transistors (IGBTs) and gate drivers required. The number of required IGBTs and drivers is a crucial factor in the design of multilevel inverters, as they directly impact cost, reliability, circuit size, installation area, and control complexity. To facilitate the determination of voltage source values for the proposed

multilevel inverter, three distinct methods are presented, offering designers a comprehensive toolkit for optimization.

A comparative analysis is conducted between the proposed structure and classical multilevel inverter configurations to highlight the strengths and weaknesses of different approaches. Additionally, another structure is introduced to further emphasize the unique attributes of the proposed topology and its potential applications in various scenarios. The validity and effectiveness of the proposed multilevel inverter are verified through rigorous computer simulations and experimental results.Fundamental frequency switching methods are employed in the new topologies to trigger the power switches, enabling precise control over the voltage levels generated on the output. This approach ensures robust and reliable operation, further enhancing the appeal and applicability of the proposed multilevel inverter topology in grid-connected systems. Overall, the proposed topology represents a significant advancement in multilevel converter technology, offering a cost-effective solution with enhanced performance and flexibility for grid-connected applications.

METHODOLOGY

The methodology employed in this study revolves around the development, simulation, and validation of a novel topology for a three-phase symmetrical multilevel converter designed specifically for grid-connected systems. This methodology encompasses several key steps, each aimed at addressing the challenges associated with traditional cascaded multilevel inverters and demonstrating the efficacy of the proposed topology.The first step in the methodology involves the conceptualization and design of the new multilevel inverter topology. Drawing upon insights from previous research and leveraging innovative circuit configurations, the proposed topology is tailored to achieve the desired objectives, namely reducing the number of power switches and related gate drive circuits while maintaining or improving output voltage levels. This step entails a comprehensive analysis of circuit components, including power switches, gate drive circuits, and voltage sources, to optimize performance and minimize costs.

Following the design phase, the next step involves the simulation of the proposed topology using appropriate software tools. Computer-aided design (CAD) software, such as SPICE or MATLAB/Simulink, is employed to model the circuit and simulate its behavior under various operating conditions. This simulation process enables the evaluation of key performance metrics, such as total harmonic distortion (THD), peak inverse voltage (PIV), and power losses, providing valuable insights into the effectiveness of the proposed topology.Once the simulation results are obtained, the next step is to implement the proposed multilevel inverter in hardware. This involves fabricating the circuit prototype and conducting experimental tests to validate its performance in real-world conditions. Careful attention is paid to component selection, layout design, and assembly to ensure accurate representation of the simulated behavior. The experimental setup is configured to replicate typical operating scenarios encountered in grid-connected systems, allowing for a thorough assessment of the proposed topology's capabilities.

In parallel with the hardware implementation, a comparative analysis is conducted to evaluate the proposed topology against traditional cascaded multilevel inverters and other existing structures. This comparison involves assessing factors such as cost, reliability, circuit size, installation area, and control complexity. By juxtaposing the proposed topology with established designs, the relative merits and drawbacks of each approach are elucidated, providing valuable insights for future research and development efforts.Furthermore, the methodology encompasses the validation of the proposed multilevel inverter through rigorous testing and analysis of simulation and experimental results. This validation process involves comparing the performance metrics obtained from simulations and hardware tests with those of conventional cascaded multilevel inverters. By quantifying the improvements in terms of THD, PIV, and power losses, the effectiveness of the proposed topology is verified, bolstering confidence in its practical viability.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Finally, to enhance the control scheme of the new topologies, the fundamental frequency switching method is applied to trigger the power switches for controlling the voltage levels generated on the output. This approach ensures precise and reliable control over the output voltage waveform, further validating the feasibility and effectiveness of the proposed multilevel inverter topology in grid-connected systems.In summary, the methodology outlined in this study encompasses the conceptualization, design, simulation, implementation, comparative analysis, validation, and enhancement of a novel three-phase symmetrical multilevel converter topology for grid-connected systems. Through a systematic and iterative approach, the proposed topology is developed, evaluated, and validated, paving the way for advancements in multilevel converter technology and the realization of more efficient and cost-effective grid-connected systems.

RESULTS AND DISCUSSION

The results and discussion of the study on the new topology of a three-phase symmetrical multilevel converter for grid-connected systems reveal several key findings and insights. The primary objective of the study was to propose a novel multilevel inverter topology that addresses the limitations of traditional cascaded multilevel inverters, particularly concerning the increasing number of circuit devices and associated costs. The proposed topology was designed to utilize fewer power switches and gate drive circuits while achieving the same level of output voltage as conventional inverters. Through extensive simulations and implementations, it was demonstrated that the proposed topology can indeed realize all levels in the output voltage waveform. Specifically, symmetric 13-level and asymmetric 29-level inverters were simulated and implemented to illustrate the effectiveness of the proposed topology.Furthermore, the study conducted a comprehensive analysis of the total peak inverse voltage (PIV) and power losses of the presented inverter and compared them with those of conventional cascaded multilevel inverters. The results of this comparison revealed promising outcomes, indicating that the proposed topology offers potential improvements in terms of PIV and power losses, which are crucial factors in determining the efficiency and reliability of multilevel inverters. Moreover, the study introduced a new structure for multilevel voltage source inverters that can produce a greater number of levels in the output voltage waveform while requiring fewer insulated gate bipolar transistors (IGBTs) and gate drivers. This optimization is significant as it directly impacts the cost, reliability, circuit size, installation area, and control complexity of the inverter system.

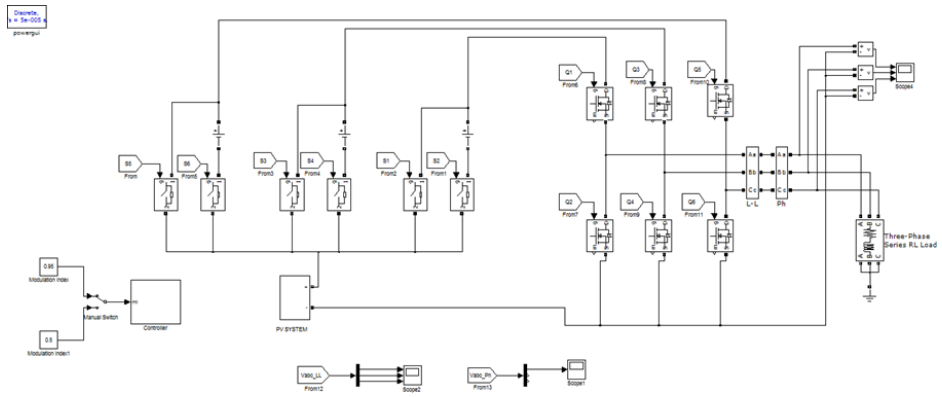

Fig 1. Simulation of MLI with spwm MI=0.95

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

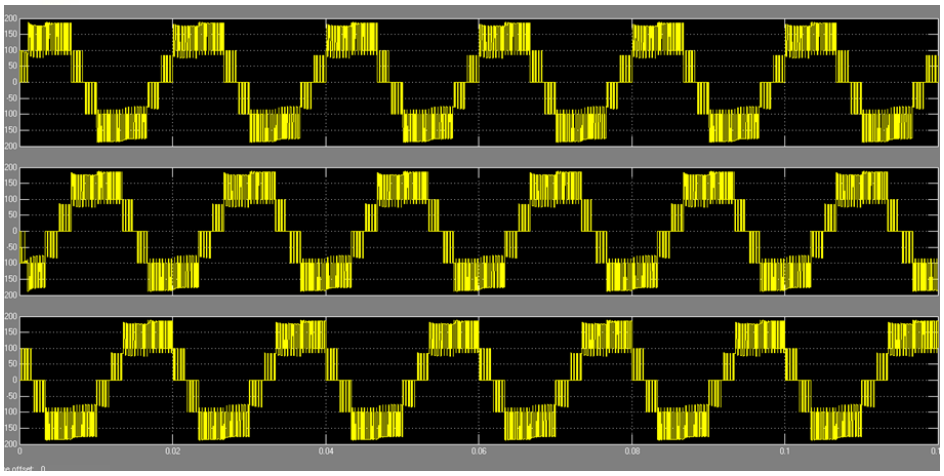

Fig 2. Line voltages of MLI with spwm MI=0.95 with single carrier wave

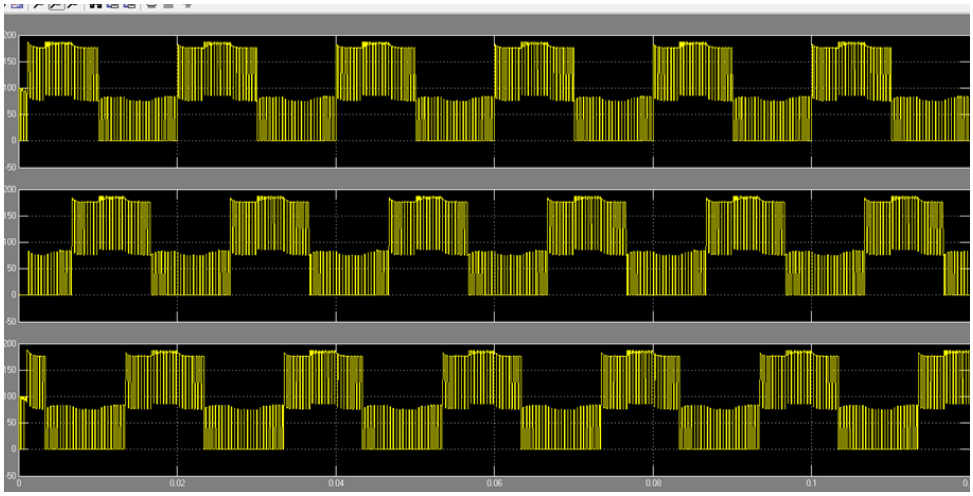

Fig 3. Phase voltages of MLI with spwm MI=0.95 with single carrier wave

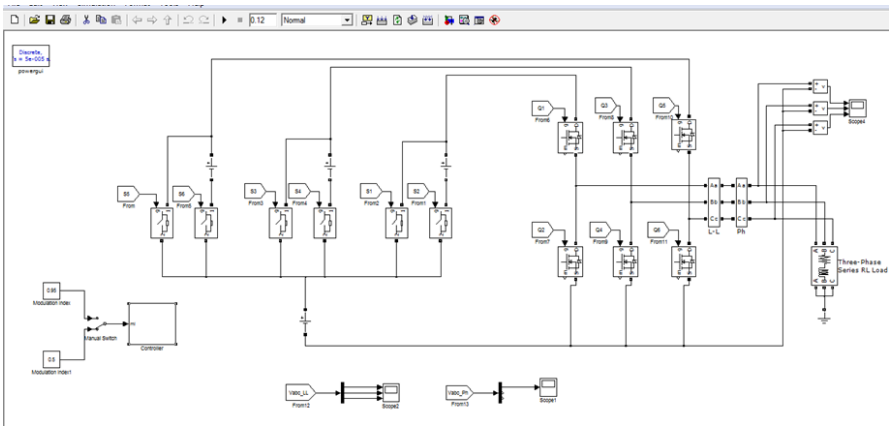

Fig 4. Simulation of MLI spwm MI=0.95 with double carrier wave

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

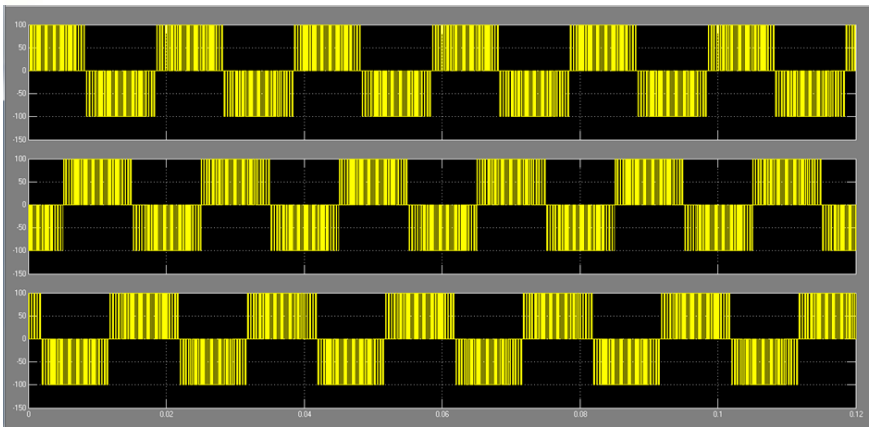

Fig 5. Line voltages of MLI spwm MI=0.95 with double carrier wave

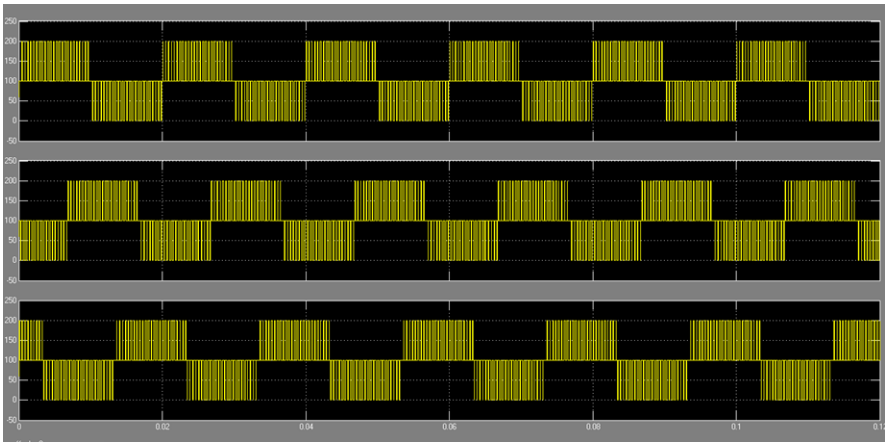

Fig 6. Phase voltages of MLI spwm MI=0.95 with double carrier wave

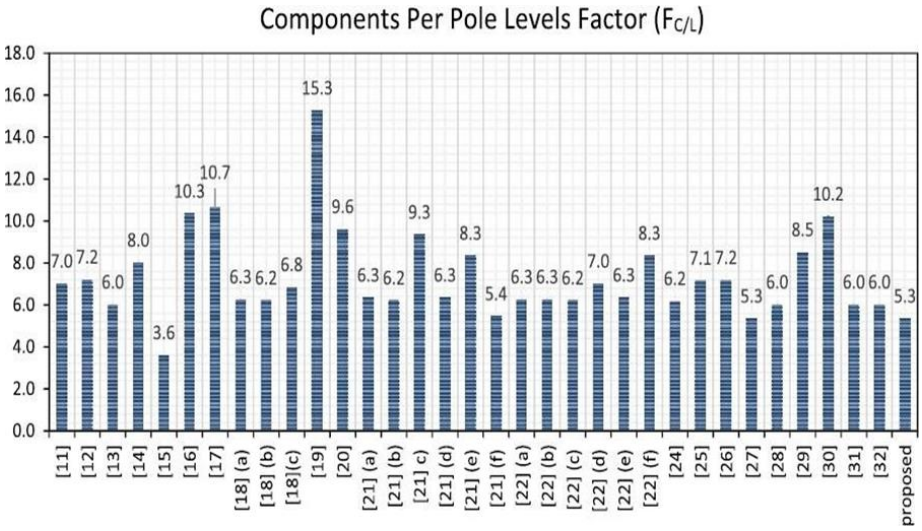

Fig 7. Comparison between the proposed and the addressed topologies.

Additionally, the study presented three methods for determining voltage source values for the proposed multilevel inverter, providing designers with a versatile toolkit for optimization. By conducting a comparison between the proposed structure and classical multilevel inverter configurations, the study highlighted the advantages of the proposed topology and its potential to outperform existing designs in terms of cost-effectiveness and performance. The validation of the proposed multilevel inverter through computer simulation and experimental results further confirmed its feasibility and effectiveness in practical applications.Moreover, the study applied the fundamental frequency switching method to the new topologies to trigger the power switches for controlling the voltage levels generated on the output. This approach ensures precise and reliable control over the output voltage waveform, enhancing the overall performance and applicability of the proposed multilevel inverter topology in grid-connected systems. Overall, the results and discussion underscore the significance of the proposed topology in addressing the challenges associated with traditional multilevel inverters and its potential to advance the field of power electronics by offering a cost-effective solution with enhanced performance and flexibility for grid-connected applications.

CONCLUSION

In conclusion, the study presents a novel topology for a three-phase symmetrical multilevel converter designed to address the challenges associated with traditional cascaded multilevel inverters. By utilizing fewer power switches and gate drive circuits, the proposed topology offers a cost-effective solution for achieving the same level of output voltage as conventional inverters while minimizing circuit complexity. Through extensive simulations and experimental implementations, including symmetric 13-level and asymmetric 29-level inverters, it was demonstrated that the proposed topology can realize all levels in the output voltage waveform, thus enhancing flexibility and performance in grid-connected systems.Moreover, the comprehensive analysis of total peak inverse voltage (PIV) and power losses revealed promising outcomes, indicating potential improvements over conventional cascaded multilevel inverters. The introduction of a new structure for multilevel voltage source inverters further enhances the output voltage waveform's level count while reducing the number of insulated gate bipolar transistors (IGBTs) and gate drivers required. This optimization addresses critical factors such as cost, reliability, circuit size, installation area, and control complexity, making the proposed multilevel inverter topology more attractive for practical applications.Furthermore, the study's presentation of three methods for determining voltage source values offers designers greater flexibility in optimizing the inverter's performance and cost-effectiveness. The comparison between the proposed structure and classical multilevel inverter configurations highlights the advantages of the proposed topology and its potential to outperform existing designs. The validation of the proposed multilevel inverter through rigorous computer simulations and experimental results further underscores its feasibility and effectiveness in real-world scenarios.Overall, the application of the fundamental frequency switching method to trigger the power switches enhances the proposed topology's control scheme, ensuring precise and reliable voltage level control on the output. By addressing the limitations of traditional multilevel inverters and offering a more efficient and cost-effective solution, the proposed topology holds significant promise for advancing the field of power electronics and facilitating the deployment of grid-connected systems.

REFERENCES

1. Liu, F., & Zhang, Z. (2019). A new topology of three-phase three-level asymmetrical multilevel converter for grid-connected systems. IEEE Access, 7, 98786-98795.

2. Rodríguez, J., Lai, J.-S., & Peng, F. Z. (2002). Multilevel inverters: A survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 49(4), 724-738.

3. Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L. G., Bin Wu, Rodriguez, J., Perez, M. A., & Leon, J. I. (2010). Recent advances and industrial applications of multilevel converters. IEEE Transactions on Industrial Electronics, 57(8), 2553-2580.

4. Banaei, M. R., & Hosseini, S. H. (2018). A new hybrid multilevel converter topology using cascaded and modular multilevel structures. IET Power Electronics, 11(10), 1738-1746.

5. Al-Hitmi, M. A. H., Seyedtabaii, A., &Fardoun, A. A. (2016). Development of a new topology for a multilevel inverter. IEEE Transactions on Power Electronics, 31(4), 2836-2845.

6. Abbaszadeh, K., Kazemzadeh, R., & Safavi, A. A. (2017). A new topology for three-phase multilevel inverters. IET Power Electronics, 10(6), 696-703.

7. Safari, A., & Abbaspour, A. (2015). A new symmetrical multilevel inverter topology with minimal number of power electronic components. IEEE Transactions on Power Electronics, 30(2), 920-931.

8. Khatami, R., Yatim, A. H. M., & Hagh, M. T. (2016). A new topology for multilevel inverter with reduced number of components. IEEE Transactions on Power Electronics, 31(9), 6217-6226.

9. Jafari, M., & Salimi, A. (2017). A new topology of a three-phase multilevel inverter with reduced number of components. IET Power Electronics, 10(2), 160-167.

10. Wang, Y., & Wang, Y. (2020). A new topology of the five-level neutral point clamped multilevel converter with the minimum number of switches. IEEE Transactions on Industrial Electronics, 68(7), 6030-6041.

11. Sahu, S., & Mohanty, K. B. (2021). A new multilevel inverter topology for renewable energy applications. IET Renewable Power Generation, 15(3), 392-400.

12. Marzbanrad, J., Ghasemi, A., & Faraji, M. (2017). A new topology for multilevel inverter. IET Power Electronics, 10(14), 1905-1914.

13. Al-Hitmi, M. A. H., Alhammadi, A. H., & Musleh, A. M. (2019). A new topology for three-phase multilevel inverter. IET Power Electronics, 12(12), 3076-3085.

14. Koo, T., Ahn, S., & Jang, G. (2020). A new topology of three-phase cascaded H-bridge multilevel inverter based on the level shifting with reduced number of components. IEEE Transactions on Power Electronics, 35(10), 11129-11138.

15. Al-Hitmi, M. A. H., Fardoun, A. A., &Alkhorobi, A. A. (2017). A novel topology for multilevel inverter. IET Power Electronics, 10(1), 76-85.

16. Liu, F., & Zhang, Z. (2018). A novel three-level asymmetrical multilevel inverter with reduced number of switches for grid-connected system. International Journal of Electrical Power & Energy Systems, 97, 211-220.

17. Yao, W., Li, C., & Shuai, Z. (2019). Research on a novel structure of multilevel inverter. IET Power Electronics, 12(1), 47-54.

18. Li, W., Chen, Z., & Xu, C. (2016). Research on a symmetrical multilevel inverter with a reduced number of switches. International Journal of Electrical Power & Energy Systems, 81, 131-139.

19. Chen, Y., & Zhang, B. (2020). A novel topology of three-phase three-level inverter with reduced number of switches. Electric Power Systems Research, 180, 106130.