International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

PERFORMANCE EVALUATION OF FAULT TOLERANT APPROXIMATE ADDER

Mrs. B. VASANTHA LAKSHMI[1], CH. JAYA SRIVANI[2], G.MADHAVI PRIYA[3], B.SAI HEMANTH[4], L.HARI ARAVIND[5], M.S.G SANKAR[6]

[1]Assistant Professor, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

The main emphasis of fault-tolerant adders is to minimize the performance metrics area, power and delay. Error resilient applications like Image processing, multimedia, and Internet of Things (IOT) accept degradation in the results providing a wide range of prospects for approximate adder's optimization. Three designs of fault-tolerant adders Selector Based Fault-Tolerant Adder-I (SBFTA-I), Selector Based Fault- Tolerant Adder-II (SBFTA-II) and Optimized Fault-Tolerant Adder (OFTA) are proposed and implemented in this project with reduced switching activity and gate count. The proposed fault tolerant adders are further used in the design of 16-bit adders, where the upper 8-bits are realized using actual adders, and the lower 8 bits are implemented using the three proposed fault tolerant adder designs.

LITERATURE SURVEY

M Priyadharshni, and Sundaram Kumaravel, "Low power and area efficient error tolerant adder for image processing application", International Journal of Circuit Theory and Applications 48(5), pp. 696-70, Wiley, 2020.

This literature describes about Approximate computing-based arithmetic units are oriented towards reduction in power, delay, and area. Intrinsic error tolerance capability of emerging application domains, like multimedia, Internet of Things (IoT), and image processing provides better opportunities for optimization of approximate arithmetic units. In this paper, a novel 1-bit imprecise full adder (IFA) is proposed with less gate count. Also, two versions of 16-bit error tolerant adders (ETAs), namely a low power and area efficient error tolerant adder (LETA) and improved low power and area efficient error tolerant adder (ILETA), are proposed. In these proposed ETAs, the most significant bit (MSB) segments are realized in same approach, whereas the least significant bit (LSB) segment of LETA and ILETA are realized using an existing modified full adder (MFA) and proposed IFAs, respectively. The proposed and existing ETA adders are implemented using a Verilog hardware description language (HDL).

Gnanambikai Palanisamy, Vijeyakumar Krishnasamy Natarajan, and Kalaiselvi Sundaram, "Area-efficient parallel adder with faithful approximation for image and signal processing applications", IET Image Processing 13(13), pp. 2587-2594, 2019.

This literature describes about, area-efficient portable complementary metal–oxide–semiconductor processors for image and signal processing applications demand reduction in transistor switching and count.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
IJARST
ISSN: 2457-0362

Adder is the fundamental block of all arithmetic operations performed in processing units. In this study, an error-tolerant parallel adder with faithful approximation is proposed that can optimise area and accuracy. In the proposed parallel adder, for n bit input and m bit adder block, least n/2m blocks are designed with approximate logic using carry by-pass addition algorithm and most n/2m blocks are designed with exact logic using carry select addition algorithm. Least significant approximate part of the adder is designed with either exact full adder (EFA) or fault-tolerant full adder (FTFA) cells. This confines the maximum error in the proposed-EFA and proposed-FTFA designs to be not more than unit bit value with weights 2[(n/2m)−1]m and 2n/2, respectively. Two different FTFA cells are proposed and implemented in the approximate blocks. The synthesis results of the proposed-EFA, proposed-FTFA1 and proposed-FTFA2 designs using Cadence Encounter with 90 nm ASIC technology for n = 16, m = 4 demonstrated an area saving of 22.3, 28.2 and 35%, respectively, when compared to the conventional counterpart.

R. Jothin, and C. Vasanthanayaki, "High Performance Significance Approximation Error Tolerance Adder for Image Processing Applications", Journal of Electronic Testing: Theory and Applications (JETTA) 32(3), pp. 377-383, 2016.

This literature describes about, Addition is one of the fundamental arithmetic operations which are used extensively in many VLSI systems such as microprocessors and application specific DSP architectures. In this paper, the Significance Approximation Error Tolerant Carry Select Adder (SAET-CSLA) is constructed, which is efficient in terms of accuracy, power and area. While considering the elementary structure of an image processing applications, it is a combination of the multipliers and delays, which in turn are the combination of the adders. This research paper describes the Algorithmic strength reduction technique which leads to a reduction in hardware complexity by exploiting the significances. This transformation is basically implemented for the reduction in the power consumption and area efficient of Very Large Scale Integration (VLSI) design or iteration period in a programmable Digital Signal Processing (DSP) implementation. The significance approximation error tolerant adder is designed using full adder and approximate full adder cells with reduced complexity at the gate level. The performance of 16 bit conventional Carry Select Adder (CSLA), 16 bit Error Tolerant carry select Adder (ET-CSLA) and proposed Significance Approximation Error Tolerant Carry Select Adder (SAET-CSLA) are compared. For all the 216 input combinations, comparison is made between existing and proposed CSLA adders and the error tolerance analysis is carried out for accuracy improvement. Application of image processing is carried out using proposed SAET-CSLA.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
IJARST
ISSN: 2457-0362

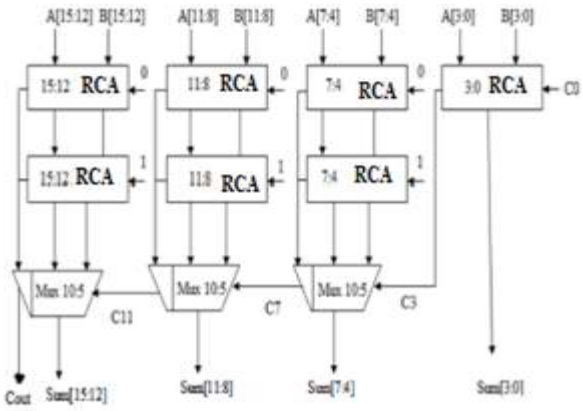


Fig.1: EXISTING METHODS

DISADVANTAGE

The problem in CSLA design is the numbers of full adders are increased then the circuit complexity also increases.

PROPOSED METHOD

To overcome the disadvantages of existing methods, two techniques has been proposed.

- Reversible Logic Gates.
- Mach Zender Interferometer technique in CLA block.

In the proposed method the carry select adder is implemented by using the mach zehnder interferometer technique in the place of cin=’0’

CARRY LOOK-AHEAD ADDER (CLA)

A Carry Look-ahead Adder (CLA) is a type of adder used in digital logic. A CLA improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit. The CLA calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

FAULT TOLERANT APPROXIMATE ADDER

Digital signal processors (DSPs) handle digital signals in error-tolerant applications. Error resilient applications like Image processing, multimedia and Internet of Things (IoT) accept degradation in the results. Approximate computing can be used to achieve abstraction on both the hardware and software levels.

The exclusion of a few algorithm levels accomplishes abstraction at the software level. Hardware-level abstraction can be achieved by altering the hardware architecture. Design engineers often face innovative techniques to improve the processor’s performance with stringent power, delay, and area constraints. Contemplating the broad range of error-resilient applications like Image processing, computer vision, multimedia processing, machine learning and Internet of Things (IoT) that accepts degradation in the results, there is a possibility to obtain improvements in these three metrics. Contemporary applications bring about a genuine tolerance with a certain amount of imprecision, although previous designs are constrained by power, area, and energy.

A vital prerequisite in designing modern computing devices is energy efficiency, which has been the driving force for chip designers to develop energy-efficient techniques to meet those requirements. The increased chip power consumption triggered by CMOS scaling becomes a significant concern in sustaining Moore’s law. Inserting the selector-based design of the fault-

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

tolerant adders reduced the switching activity resulting in reduced area and power in proposed methods.

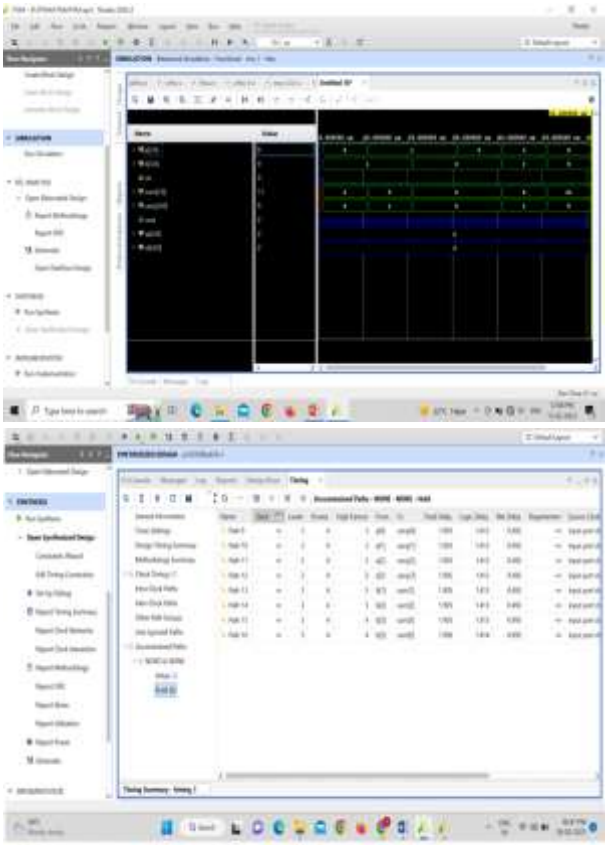
DESIGNING FTAA:

CSLA's higher power and area make them incompatible with portable devices owing to hardware complexity, despite being one of the fastest adders. The CSLA's used in the present scenario use RCA's for the concurrent calculation of the sum when the carry bit is one and zero. The output is determined by a multiplexer depending on the previous carry. Consequently, part of the RCA's remains continuously functioning, leading to enhanced power dissipation and area. The incorporation of approximate computing in the CSLA can reduce the hardware complexity.

This is obvious from Table I where there is a reduction in the counts of gates and the gate delay for the sum and carry of the proposed adders in comparison to the existing approximate adders. Significant savings in power, delay and area can be achieved by using approximate computing by compromising the precision of the outputs. The vital element in constructing an approximate circuit is to minimize the hardware and carry propagation delay. Some error results are allowed in the output of a complex circuit to simplify the logic expressions, thereby reducing the logic counts.

Arithmetic units based on approximate computing are tailored towards power, delay, and area reduction. Three designs of fault tolerant approximate adders are designed and proposed by optimizing the power, area, and delay in this work. The designs are Selector Based Fault Tolerant Adder-I (SBFTA-I), Selector Based Fault Tolerant Adder-II (SBFTA-II) and Optimized Fault Tolerant Adder (OFTA). The existing and proposed designs of approximate adders are compared in terms of sum and carry Boolean expressions, gate count, gate delay in sum and carry.

SIMULATION RESULTS



CONCLUSION

In this project, we have introduced a fault tolerant approximate adder with is designed using the SBFTA-I or SBFTA-II or OFTA which are generally made up of gates and multiplexers, and very less no. of XOR

gates. The architecture of the Fault Tolerant approximate adder modules were performed using under the Xlinx-2022.2 Vivado, the VHDL coding language.

The simulation, design implementation, and analytical outcomes obtained from waveforms were tested for the approximate addition with some faulty inputs. The proposed module plays the important and significant role to study further for designing and implementation of the CSLA for the their application in the FPGA kit.

REFERENCES

1. M Priyadharshni, and Sundaram Kumaravel, "Low power and area efficient error tolerant adder for image processing application", International Journal of Circuit Theory and Applications 48(5), pp. 696-70, Wiley, 2020.
2. Gnanambikai Palanisamy, Vijeyakumar Krishnasamy Natarajan, and Kalaiselvi Sundaram, "Area-efficient parallel adder with faithful approximation for image and signal processing applications", IET Image Processing 13(13), pp. 2587-2594, 2019.
3. R. Jothin, and C. Vasanthanayaki, "High Performance Significance Approximation Error Tolerance Adder for Image Processing Applications", Journal of Electronic Testing: Theory and Applications (JETTA) 32(3), pp. 377-383, 2016.
4. R. Jothin, and C. Vasanthanayaki, "High performance error tolerant adders for image processing applications", IETE Journal of Research. pp. 1-12, 2018.
5. Sunil Dutt, S ukumar Nandi, and Gaurav Trivedi, "Analysis and Design of Adders for Approximate Computing", ACM Transactions on Embedded Computing Systems, Vol. 17, No. 2, 2017.
6. M. Priyadharshni, Antra Raj Gupta, V. Nithish Kumar, and S. Kumaravel, "An error efficient and low complexity approximate multibit adder for image processing applications", International Journal of Circuit Theory and Applications, 49(8), pp. 2373-2381, 2021.
7. Hyoju Seo, Yoon Seok Yang and Yongtae Kim, "Design and Analysis of an Approximate Adder with Hybrid Error Reduction", Electronics, 9(3), 471, 2020.