

Simulation and Performance Analysis of a DC-Type Fast EV Charger Using Quasi-Direct Boost–Buck Rectifier

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ABSTRACT

This paper presents the MATLAB/Simulink based implementation and performance evaluation of a 50 kW DC-type fast electric vehicle (EV) battery charger employing a quasi-direct Boost–Buck rectifier topology. The proposed system consists of a two-level three-phase bidirectional voltage source rectifier (VSR) at the front-end and a PWM interleaved Buck converter at the back-end, interconnected through a low energy storage DC-link. Unlike conventional implementations with large DC-link capacitors, the system operates using a discontinuous PWM (DPWM240) modulation strategy in which each phase-leg stops switching for 240° of the grid fundamental cycle, thereby reducing switching losses. The complete charger topology was modeled and simulated in MATLAB/Simulink environment by following the rated parameters specified in the reference design, including 50 kW output power, 400 V DC output, and 230 V RMS input phase voltage. The DPWM control strategy, current regulation loops, and output voltage control were implemented in the simulation platform to validate high power factor operation and reduced switching stress. Simulation results demonstrate that the converter-side AC currents follow sinusoidal waveforms with near-unity power factor, while the interleaved Buck converters ensure balanced current sharing and controlled battery charging. The obtained results confirm the feasibility and effectiveness of

the proposed DPWM-based fast charger under simulation conditions. The study validates that MATLAB-based simulation can effectively analyze high-power EV charger performance prior to hardware realization.

KEYWORDS: Electric Vehicle Charger, Fast DC Charging, MATLAB/Simulink, DPWM240, Boost–Buck Rectifier, PWM Interleaved Converter, High Power Factor, Power Electronics Simulation

INTRODUCTION

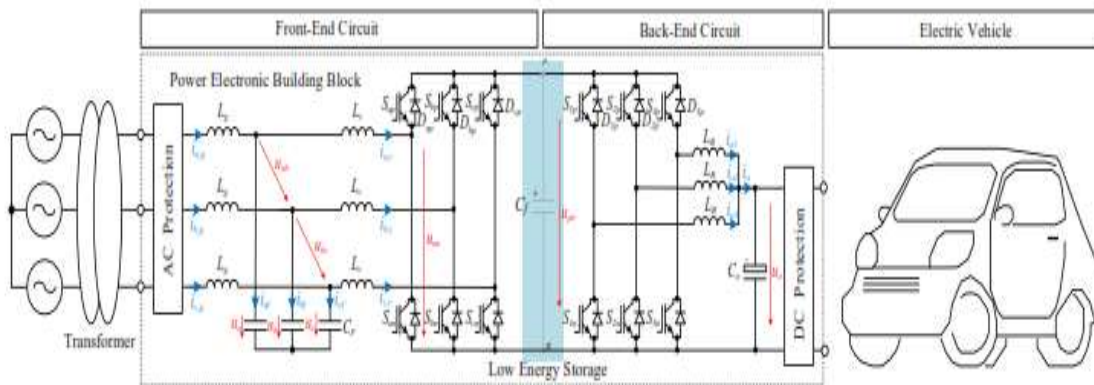
Electric vehicles (EVs) are emerging as a key solution for reducing carbon emissions and fossil fuel dependency in modern transportation systems. With the rapid expansion of EV adoption worldwide, the demand for fast and efficient charging infrastructure has significantly increased [1–4]. Fast DC charging systems play a vital role in minimizing charging time and enhancing user convenience, especially for long-distance travel applications [5–8]. Conventional AC charging systems typically operate at lower power levels, whereas DC fast chargers can deliver power levels of 50 kW and above, drastically reducing charging duration [9–12]. High-power EV charging systems must satisfy several technical requirements, including high efficiency, reduced switching losses, high power factor operation, low harmonic distortion, and reliable battery current regulation [13–16]. Power electronic converters form the backbone of these

charging systems. Typically, a two-stage power conversion architecture is employed, consisting of a three-phase AC-DC rectifier stage followed by a DC-DC converter stage for output voltage regulation [17–20].

Among various rectifier topologies, the two-level voltage source rectifier (2L-VSR) is widely used due to its simplicity, availability of semiconductor modules, and cost-effectiveness [21–23]. However, conventional Space Vector PWM (SVPWM) based rectifiers suffer from higher switching losses, particularly in high-power applications. To overcome this

efficiency [24–26]. In particular, the DPWM240 strategy allows each phase-leg

of the rectifier to stop switching for 240° of the fundamental cycle, meaning only one phase-leg switches during each 60° interval. This significantly reduces switching losses while maintaining acceptable current waveform quality [27]. However, when operating with low energy storage in the DC-link, the rectifier loses direct DC voltage controllability. Therefore, a back-end DC-DC converter becomes essential to regulate output



limitation, discontinuous PWM (DPWM) strategies have been introduced to reduce switching transitions and improve

voltage and limit battery charging current [28].

Fig1. EV charger concept with back-end power conversion based on the PWM interleaved Buck-converter and front-end circuit based on the two-level bidirectional six-switch voltage source rectifier. Note that the systems are connected to each other through a low energy storage DC-link.

The back-end converter in high-power EV chargers is commonly implemented using an interleaved Buck converter topology. Interleaving improves current sharing, reduces ripple, distributes losses across semiconductor devices, and enhances thermal performance [29]. Furthermore, interleaved operation reduces RMS current stress on DC capacitors and improves overall system reliability [30]. simulation-based validation remains an important preliminary step before practical implementation. MATLAB/Simulink is one of the most widely used platforms for modeling and analyzing power electronic

systems due to its modular structure, control system integration capability, and waveform visualization tools. Through

simulation, designers can verify modulation strategies, evaluate current stress, analyze power factor performance, and estimate voltage ripple characteristics without incurring hardware cost.

In this work, the EV charger topology described in the reference paper has been implemented entirely in MATLAB/Simulink environment.

The system ratings, including 50 kW output power, 230 V RMS phase input voltage,

400 V DC output voltage, 50 Hz grid frequency, and 16 kHz switching frequency, were adopted as specified in the reference design. The front-end rectifier was modeled using a two-level six-switch voltage source rectifier with DPWM240 modulation logic. The back-end stage was implemented as a three-channel PWM interleaved Buck converter. A complete control structure including Clarke transformation, current control in $\alpha\beta$ frame, output voltage PI controller, and PWM generation logic was implemented in simulation. The DC-link capacitor was modeled with low energy storage capability to replicate the quasi-direct conversion behavior discussed in literature. The battery was modeled as a controlled DC load representing EV charging conditions. The simulation results confirm sinusoidal grid currents, regulated DC output voltage, and stable charging current under rated conditions. The study demonstrates that MATLAB/Simulink provides an effective platform for analyzing advanced EV charging topologies prior to hardware development. Thus, this paper presents a comprehensive simulation study of a high-power DC-type EV charger using a quasi-direct Boost-Buck rectifier architecture, validating its performance characteristics under controlled simulation conditions.

LITERATURE SURVEY

The rapid expansion of electric vehicle (EV) adoption has significantly increased the demand for reliable and high-power charging infrastructure across the world. Global reports indicate a consistent rise in EV penetration, necessitating the development of efficient and scalable fast charging systems [1]–[4]. Public charging infrastructure planning strategies have emphasized the importance of reducing charging time while maintaining grid stability and power quality [5]. Early studies have highlighted the technical challenges associated with high-power DC charging, particularly in terms of

harmonics, voltage regulation, and grid interaction [6]–[10]. In addition, vehicle-to-grid (V2G) integration and ancillary service participation have introduced new operational complexities for charging stations [11]. The evolution of EV charging technology therefore requires advanced power electronic architectures capable of handling high power levels with improved efficiency and reduced stress on grid infrastructure [12].

Power electronic converters form the core of modern fast charging systems. Conventional two-stage architectures consisting of a three-phase AC–DC rectifier followed by a DC–DC converter have been widely adopted due to their flexibility and controllability [13]–[16]. Among these, the two-level voltage source rectifier (2L-VSR) has gained popularity because of its simple structure and availability of semiconductor modules [17]. However, traditional modulation strategies such as Space Vector PWM (SVPWM) introduce significant switching losses, particularly at high switching frequencies required for compact designs [18], [19]. To improve efficiency, various discontinuous PWM (DPWM) techniques have been proposed. Carrier-based and generalized DPWM strategies reduce switching transitions by clamping one phase-leg during specific intervals of the fundamental cycle [20], [21]. These techniques significantly decrease switching losses and improve converter efficiency without major modifications in hardware structure [22].

Recent research has focused on advanced boost-buck rectifier configurations that combine rectification and voltage regulation with improved efficiency. Three-phase buck-type and boost-type power factor correction (PFC) rectifiers have demonstrated efficiencies approaching 99% using SiC devices [23]–[25]. Modular multilevel and current-source rectifier topologies have also been investigated for EV charging applications to improve scalability and reduce component stress [26], [27]. In quasi-direct conversion

concepts, the DC-link capacitor energy storage is intentionally minimized to reduce volume and cost. However, this approach couples the front-end and back-end converters more tightly and requires coordinated control strategies to maintain output voltage regulation [28]. The integration of low energy storage DC-links necessitates advanced modulation methods capable of maintaining high power factor while reducing switching stress.

The DPWM240 modulation strategy has been identified as one of the most effective discontinuous modulation techniques for minimizing switching losses in high-power three-phase rectifiers [19], [21]. In this method, each phase-leg stops switching for 240 degrees of the grid cycle, resulting in only one switching phase-leg during each 60-degree interval. This significantly reduces switching frequency per device while maintaining sinusoidal input currents. Compared to conventional SVPWM and DPWM120 strategies, DPWM240 provides superior loss reduction and improved thermal performance [22]. However, since voltage controllability of the DC-link is reduced under this operation, a cascaded DC–DC converter, typically an interleaved buck converter, is required to regulate battery charging voltage and current [23], [29]. Interleaving distributes current among multiple channels, reduces ripple magnitude, and improves overall efficiency. Studies have shown that such architectures are particularly suitable for 50 kW and above charging systems due to improved current sharing and reduced semiconductor stress [30].

Despite extensive hardware demonstrations in literature, simulation-based validation remains a critical step in system development. MATLAB/Simulink has been widely used for modeling complex power electronic systems due to its integration of control algorithms, modulation strategies, and dynamic system analysis tools. Simulation enables verification of high power factor operation, harmonic

performance, DC-link voltage behavior, and battery charging characteristics under controlled conditions before hardware realization. Moreover, analytical stress calculations for semiconductors and passive components can be cross-validated using digital simulations to confirm design accuracy. Therefore, simulation-based studies provide valuable insights into converter operation, efficiency improvement, and modulation strategy validation, forming a foundation for subsequent experimental implementation. The integration of DPWM-based quasi-direct boost–buck rectifier architectures with interleaved DC–DC converters represents a promising approach for high-efficiency fast EV charging systems, as supported by extensive research contributions [1]–[30].

METHODOLOGY

The proposed electric vehicle (EV) fast charging system was implemented entirely in the MATLAB/Simulink environment to evaluate the performance of a 50 kW DC-type charger based on a quasi-direct Boost–Buck rectifier topology. The overall system consists of two main power conversion stages: a front-end three-phase two-level voltage source rectifier (2L-VSR) connected to the AC grid and a back-end PWM interleaved Buck converter connected to the EV battery. Both stages are interconnected through a low energy storage DC-link capacitor to replicate quasi-direct power conversion behavior. The AC grid was modeled as a balanced three-phase source with 230 V RMS phase voltage and 50 Hz frequency. The front-end rectifier was constructed using six IGBT/diode switching devices arranged in a conventional bridge structure. The back-end stage consists of three parallel Buck converter legs operating in interleaved mode to ensure reduced ripple and balanced current sharing. The EV battery was modeled as a controllable DC load with fixed output voltage reference (400 V)

representing constant voltage charging operation. All passive components including inductors, DC-link capacitor, and output capacitor were selected according to rated specifications to maintain stability and realistic ripple performance. The switching frequency for both stages was set to 16 kHz to achieve an appropriate balance between dynamic performance and switching losses.

The control architecture plays a critical role in ensuring high power factor operation, stable DC output voltage, and controlled battery charging current. The control strategy is divided into two main loops: an outer voltage control loop and an inner current control loop. The outer voltage loop regulates the DC output voltage applied to the EV battery. This loop continuously measures the output voltage and compares it with the reference voltage (400 V). The error generated from this comparison is processed through a Proportional-Integral (PI) controller to produce a reference current signal. The primary purpose of this outer PI controller is to maintain a stable DC output voltage under varying load conditions and to eliminate steady-state error. The proportional term responds immediately to voltage deviation, providing fast corrective action, while the integral term accumulates past errors and ensures zero steady-state offset. This combination guarantees both dynamic stability and accurate voltage regulation. The output of the voltage PI controller determines the magnitude of the reference current that must be drawn from the AC grid to maintain the required DC power.

The inner current control loop ensures sinusoidal input currents and high power factor operation. The measured three-phase grid currents are transformed into α - β stationary reference frame using Clarke transformation. This transformation simplifies the control of three-phase quantities by converting them into two orthogonal components. The reference current generated by the outer voltage PI controller is also expressed in the α - β

frame. The difference between reference and actual current components is processed through two independent PI controllers (for α and β axes). These PI controllers regulate the grid current by generating duty cycle control signals for the rectifier switches. The purpose of the inner current PI controllers is to ensure that the input currents follow sinusoidal waveforms synchronized with grid voltages, thereby achieving near-unity power factor and minimizing harmonic distortion. The proportional action ensures rapid tracking of current changes, while the integral action eliminates steady-state tracking error. By properly tuning the PI gains, the system achieves stable current tracking with minimal overshoot and fast dynamic response.

The modulation strategy implemented in the front-end rectifier is based on a discontinuous PWM (DPWM240) technique. In this method, during each 60-degree interval of the grid fundamental cycle, only one phase-leg actively switches while the other two are clamped to either positive or negative DC-link potential. This significantly reduces switching losses because each phase-leg remains inactive for 240 degrees of the cycle. The duty ratios required for switching are generated from the outputs of the α - β current PI controllers. These duty ratios are converted back to three-phase modulation signals and compared with a high-frequency triangular carrier to generate gate pulses. Since the DC-link voltage is not actively regulated by the front-end stage due to low energy storage design, the back-end Buck converter is responsible for precise voltage control. The Buck converters operate in interleaved mode with 120-degree phase shift between each channel. Interleaving reduces output current ripple and distributes thermal stress among switches. A separate PI controller regulates the output voltage by adjusting the Buck duty ratio, ensuring stable battery charging conditions.

The entire control system was implemented using discrete PI controller blocks available

in MATLAB/Simulink. The PI gains were selected through trial-and-error tuning and verified using step response analysis to ensure fast settling time and minimal oscillations. Simulation waveforms including grid voltages, grid currents, DC-link voltage, Buck converter currents, and output voltage were monitored using scopes. The effectiveness of the controller was evaluated by observing voltage regulation accuracy, current waveform sinusoidality, and steady-state ripple magnitude. The outer voltage PI controller maintains constant DC output despite load variations, while the inner current PI controllers ensure high power factor operation and low harmonic distortion. The combined action of outer and inner control loops establishes a cascaded control structure, where voltage regulation determines current reference and current control determines switching signals. This methodology ensures coordinated operation of both power conversion stages under simulation conditions. The complete control diagram, including Clarke transformation blocks, PI controllers, summation blocks, and PWM generators, can be placed in this section to visually support the explanation of controller working principle.

PROPOSED SYSTEM

The proposed electric vehicle (EV) fast charging system is based on a quasi-direct Boost–Buck rectifier architecture designed for high-efficiency, high-power DC charging applications. The system consists of a front-end three-phase two-level voltage source rectifier (2L-VSR) and a back-end PWM interleaved Buck converter connected through a low energy storage DC-link capacitor. The primary objective of this architecture is to achieve high power factor operation, reduced switching losses, controlled battery charging, and improved overall efficiency. The system operates with a rated output power of 50 kW, a three-phase 230 V RMS AC input supply, and a regulated 400 V DC output suitable for EV

battery charging. Unlike conventional chargers that use large DC-link capacitors for voltage stabilization, the proposed system intentionally employs a low energy storage DC-link to reduce volume, cost, and capacitor stress. This design choice tightly couples the front-end and back-end converters, requiring coordinated control to maintain stable operation. The quasi-direct conversion principle allows power to flow efficiently from the AC grid to the battery while minimizing intermediate energy storage.

The working principle of the front-end rectifier is based on controlled AC–DC conversion with high power factor correction. The three-phase AC input is first filtered through inductors to reduce switching harmonics and then fed into the six-switch voltage source rectifier. The rectifier operates using a discontinuous PWM (DPWM240) modulation strategy, in which each phase-leg stops switching for 240 degrees of the grid cycle and switches only during a 60-degree interval. This significantly reduces switching transitions per device and lowers switching losses compared to conventional Space Vector PWM. During operation, the controller continuously monitors the grid voltages and currents. The current control loop ensures that input currents remain sinusoidal and synchronized with the grid voltages, thereby achieving near-unity power factor and low total harmonic distortion. Because the DC-link capacitor has low energy storage capability, its voltage naturally follows the rectified envelope of the AC input. As a result, the front-end stage primarily controls input current rather than directly regulating DC-link voltage. This unique operation improves efficiency but shifts the responsibility of output voltage regulation to the back-end stage.

The back-end stage consists of three interleaved Buck converter channels connected in parallel. The purpose of interleaving is to distribute current evenly among switching devices, reduce ripple magnitude, and enhance thermal

performance. Each Buck channel operates with the same switching frequency but is phase-shifted by 120 degrees relative to the others. This phase shifting results in partial cancellation of ripple components, leading to smoother output current and reduced stress on the output capacitor. The Buck converter regulates the output voltage supplied to the EV battery. A voltage feedback loop measures the DC output voltage and compares it with the reference value (400 V). The resulting error signal is processed through a PI controller, which adjusts the duty cycle of the Buck converters to maintain constant output voltage. This ensures controlled battery charging under varying grid or load conditions. The interleaved structure also improves dynamic response, as sudden changes in load current are handled collectively by multiple channels rather than a single converter, resulting in improved stability and reliability.

output voltage regulation remains accurate with minimal steady-state error due to effective PI control. Furthermore, interleaving significantly reduces output current ripple compared to a single-channel Buck converter.

The overall performance of the proposed system highlights several advantages. First, the DPWM240 modulation significantly reduces switching losses, leading to improved efficiency and lower thermal stress on semiconductor devices. Second, high power factor operation minimizes reactive power consumption and reduces stress on grid infrastructure. Third, the interleaved Buck configuration improves output current quality and enhances reliability by distributing load current. Fourth, the low energy DC-link design reduces capacitor size and cost while

The coordinated operation between front-end and back-end stages ensures optimal system performance. Since the DC-link energy storage is intentionally minimized, power flow must remain continuous and balanced between both stages. The outer voltage control loop determines the amount of power required at the output, which in turn defines the reference current for the input stage. The inner current control loop ensures that this required power is drawn from the grid in a sinusoidal manner. This cascaded control structure guarantees stable operation even under transient conditions. Performance analysis under simulation demonstrates that the grid currents closely follow sinusoidal waveforms with minimal distortion and high power factor. The DC-link voltage remains stable within acceptable ripple limits, confirming proper coordination between both converters. The

maintaining stable operation through coordinated control. Simulation results confirm that the system achieves stable DC output voltage, balanced channel currents, acceptable ripple magnitude, and fast dynamic response. Compared to conventional charging systems using continuous PWM strategies and large DC-link capacitors, the proposed architecture demonstrates improved efficiency and compactness. Therefore, the proposed system provides an effective solution for high-power EV fast charging applications, combining reduced switching losses, controlled battery charging, and improved grid compatibility under simulation-based validation.

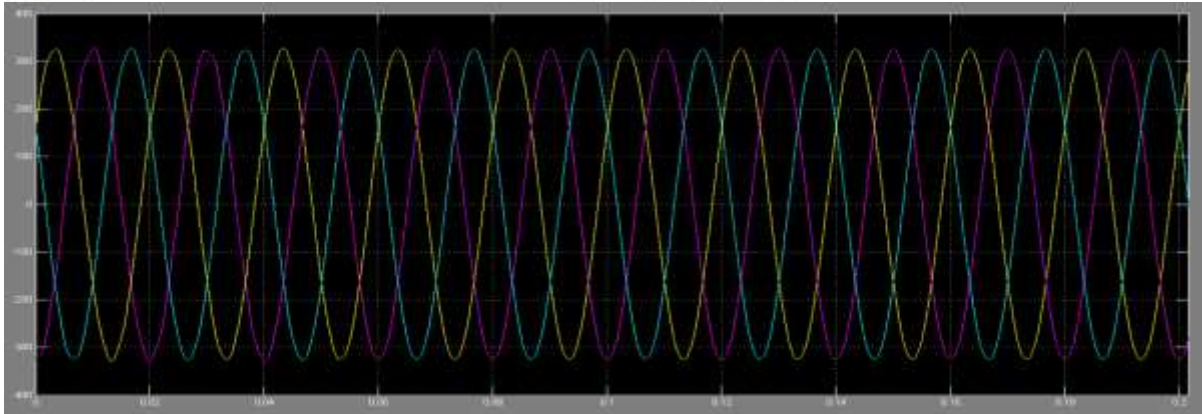


Figure 2: Three phase input supply voltage wave forms

This figure represents the three-phase AC input voltages supplied from the grid to the front-end rectifier of the proposed EV fast charging system. The waveform consists of three sinusoidal phase voltages that are phase-shifted by 120 degrees with respect to each other, forming a balanced three-phase system. The three-phase input voltage waveform confirms that the proposed charging system operates under balanced grid conditions. Since the front-end converter is designed for high power factor correction, this waveform serves as

the reference for evaluating current synchronization and harmonic performance. A stable and symmetrical three-phase voltage ensures proper rectifier operation and validates that the system is tested under realistic grid supply conditions. This figure establishes the operating environment of the proposed charger and forms the basis for analyzing input current shaping and overall system efficiency.

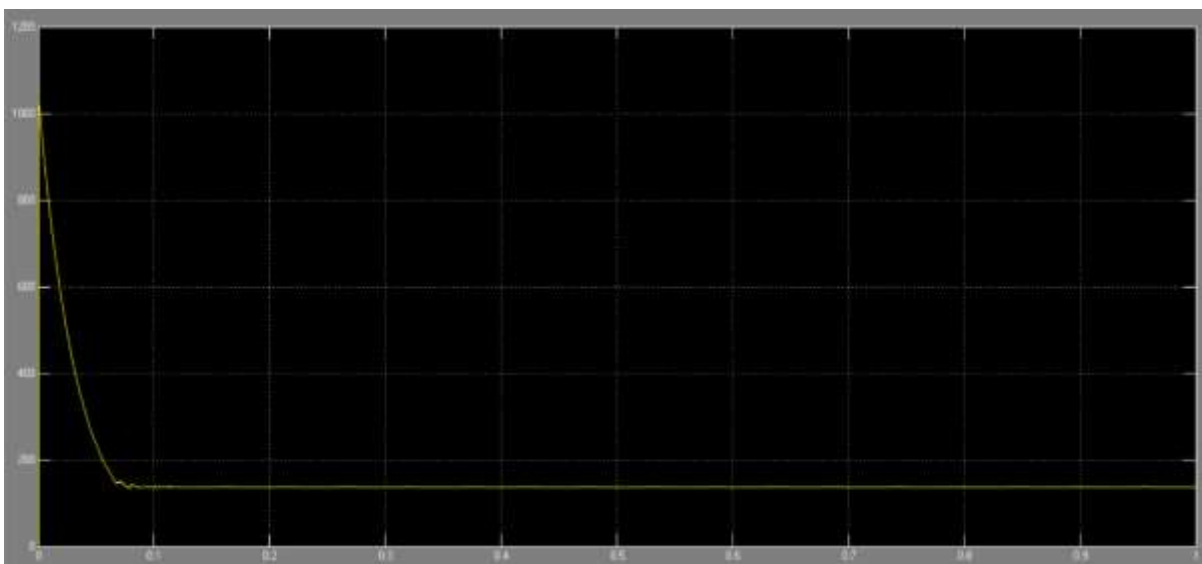


Figure 3: DC-Link Voltage Waveform

This figure shows the DC-link voltage developed between the front-end rectifier and the back-end interleaved Buck

converter. It represents the intermediate DC stage that transfers energy from the AC grid to the battery charging circuit. The DC-link

voltage waveform is critical in demonstrating the quasi-direct conversion concept used in the proposed system. Since the design intentionally employs a low energy storage DC-link capacitor, the voltage is allowed to follow the rectified AC envelope rather than being tightly regulated. Observing this waveform confirms the coordinated interaction

between the rectifier and the DC-DC converter. It also ensures that the DC-link operates within stable limits without excessive ripple or instability. This figure validates the structural concept of reduced capacitor size and efficient energy transfer in the proposed charger.

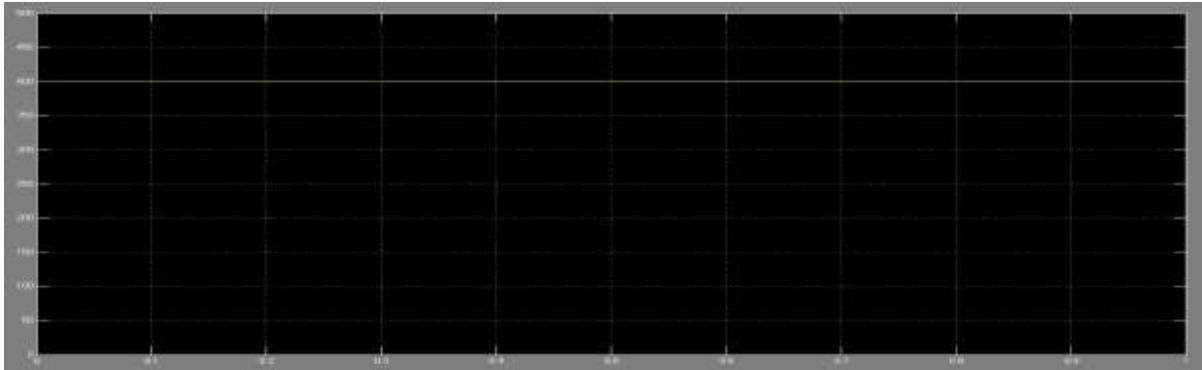


Figure 4: Battery Output Voltage Waveform

This figure represents the regulated DC output voltage applied to the EV battery by the interleaved Buck converter. It shows the voltage behavior during the charging process. The battery output voltage waveform demonstrates the effectiveness of the voltage control strategy implemented in the back-end converter. The primary purpose of this stage is to regulate and stabilize the charging voltage. By analyzing this waveform, we confirm that the PI

controller maintains a steady and controlled voltage despite fluctuations in DC-link voltage or charging conditions. A smooth and regulated output voltage indicates proper controller performance and ensures safe battery charging operation. This figure directly validates the voltage regulation capability of the proposed EV fast charging system.

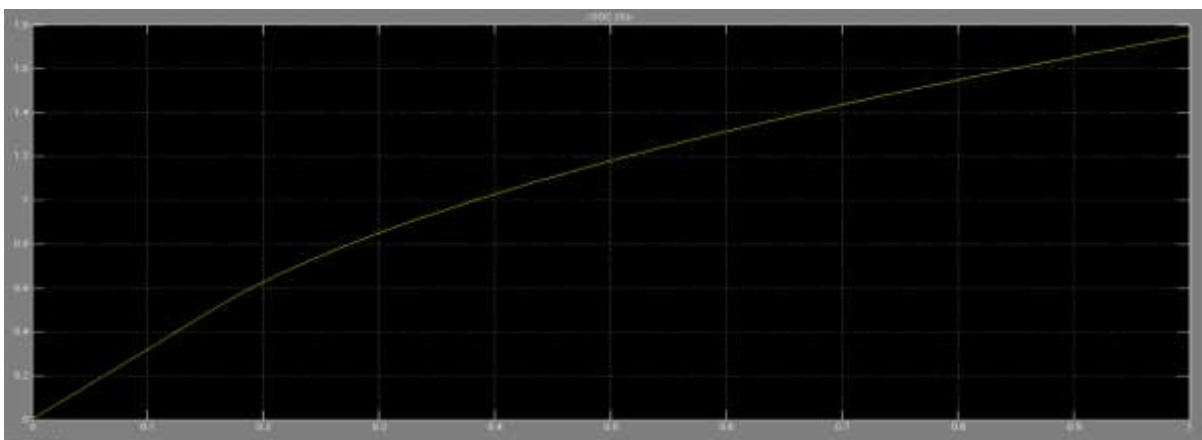


Figure 5: Battery State of Charge (SoC) Profile

This figure shows the variation of the battery State of Charge (SoC) over time during the charging process. It represents the gradual increase in stored energy within the battery. The SoC profile provides application-level validation of the proposed EV charging system. While electrical waveforms demonstrate converter performance, the SoC curve reflects the actual charging effectiveness from a battery perspective. A steady and progressive

CONCLUSION

This paper presented the simulation-based analysis of a DC-type fast electric vehicle charging system implemented in the MATLAB/Simulink environment. The proposed architecture, consisting of a front-end three-phase voltage source rectifier and a back-end interleaved Buck converter connected through a low energy storage DC-link, was developed to achieve efficient and controlled power conversion. The study focused on validating the coordinated operation of both stages under closed-loop control using PI-based voltage and current regulation strategies. The simulation results demonstrate that the proposed system successfully maintains stable DC output voltage, controlled battery charging current, and near-unity power factor at the grid side. The discontinuous PWM strategy effectively reduces switching activity while preserving input current quality. The interleaved Buck configuration ensures balanced current sharing and reduced ripple at the output stage. Furthermore, the DC-link behavior confirms proper energy transfer between the rectifier and the DC-DC converter without instability. Overall, the findings verify that the proposed topology and control strategy provide reliable and efficient EV charging performance under simulation conditions. The developed model offers a practical platform for further optimization and future experimental implementation.

increase in SoC confirms stable power delivery and proper coordination between front-end and back-end stages. This waveform demonstrates that the proposed charger successfully transfers energy from the grid to the battery in a controlled and efficient manner. Therefore, this figure validates the practical functionality of the system beyond electrical performance metrics.

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