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### Convolution and Deconvolution Application using Ancient Indian Vedic Mathematics

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**Abstract:** Convolution and Deconvolution is having wide area of application in Digital Signal Processing. As in DSP Convolution and Deconvolution of long sequences is often required in many applications. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Primary requirement of any application to work fast is that increase the speed of their basic building block. Multiplier and Divider is the heart of convolution and Deconvolution respectively. It is most important but, slowest unit of the system and consumes much time in the system. Many methods are invented to improve the speed of the Multiplier and Divider, amongst all vedic Multiplier and Divider is under focus. Because, of faster working and low power consumption. In this paper the speed of Convolution and Deconvolution module is increased using Vedic multiplier and Divider.

**Keywords:** Linear Convolution, Deconvolution, Vedic Mathematics, UrdhvaTiryagbhyam Sutra, Paravartya Sutra, Nikhilam Sutra.

#### I. INTRODUCTION

With continuous advancement in VLSI technology, Need of high speed convolution and Deconvolution is required. as many areas of Electrical and Electronics Engineering, Digital signal processing plays an important role, Discrete Convolution and Deconvolutionis having extreme importance in Digital signal processing. Convolution is having wide area of application like designing the digital filter, correlation etc. However it is quite difficult for the new candidate to perform convolution as convolution method is so lengthy and time consuming. So many methods are proposed for performing Discrete Convolution, one of a tough approach is a Graphical method, it is quite sophisticated and systematic but, it is very lengthy and time consuming. The main module for performing Convolution and Deconvolution is Multiplier and Divider. Pierre and John have implemented the fast method for performing linear convolution. This method is very easy; it is like to perform simple multiplication of Decimal numbers. And because of this method in very little time it is possible to calculate Convolution of long sequences is very easily. Also a Novel method is used for performing Deconvolution.

This method is similar to calculate long division and polynomial division. As Adder is also an important block for the proposed method, so all the possible adders is studied and synthesized using Altera Quartus II design suit. The Delay and Area of all adders is compared. Amongst all Adder which having highest speed and occupy less area is used for performing convolution. For the conventional multiplication, multipliers with Traditional shifts and add method is used. This method is difficult for VLSI implementation and also its Delay is too large. Vedic mathematics provides the unique solution for Multiplication and Division. Vedic Multiplier based on urdhavatiryagbhyam sutra (Vertically and Crosswise) is used to implement Convolution. For Deconvolution various Divider is Studied, by comparing the advantages and disadvantages of each method, Divider using Paravartya Sutra is used for implementation.

#### **II. VEDIC MATHEMATICS**

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. We must be thankful to Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics and acknowledge the work of various people regarding Vedic Mathematics. Vedic mathematics is mainly based on 16 Sutras. These sutras along with their brief meaning are enlisted below alphabetically.

- AnurupyeShunyamanyat– If one is in ratio, the other is zero.
- Chalana-Kalanabyham– Differences and Similarities.
- **EkadhikinaPurvena** By one more than the previous one.
- **EkanyunenaPurvena** By one less than the previous one.
- **Gunakasamuchyah-** The Factor of the sum is equal to the sum of Factor.
- **Gunitasamuchyah-** The product of sum is equal sum of product.



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- NikhilamNavatashcaramamDashatah– All from 9 and the last from 10.
- ParaavartyaYojayet- Transpose and adjust.
- **Puranapuranabyham**–By the completion or noncompletion.
- Sankalana-vyavakalanabhyam– By addition and by subtraction.
- ShesanyankenaCharamena– The remainders by the last digit.
- ShunyamSaamyasamuccaye–When the sum is the same that sum is zero.
- **Sopaantyadvayamantyam** The ultimate and twice the penultimate.
- UrdhvaTiryagbyham- Vertically and crosswise.
- Vyashtisamanstih– Part and Whole.
- Yaavadunam-Whatevertheextenttofits deficiency.

#### **III. CONVOLUTION METHOD**

Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal. Convolution helps to estimate the output of a system with arbitrary input, with knowledge of impulse response of the system. Linear systems characteristics are completely specified by the systems impulse response, as governed by the mathematics of convolution. Convolution is an operation which takes two functions as input, and produces a single function output (much like addition or multiplication of functions) The

		y(n)	=	f(n	) * g(n)	n)			
	y(n)	=	$\sum_{k=-\infty}^{\infty}$	f(k)	g(n -	(k)			
x(n):		~	4	5	3	1			
h(n):			2	7	9	3			
			8	10	6	2			_
				28	35	21	7		
					36	45	27	9	
						12	15	9	3
Y(n):			8	38	77	80	49	18	3
a 1	<b>C</b> (	р.		C			1		

Convolution of two Discrete Sequences is given by

#### Fig.1. Convolution by Proposed Method.

Consider the example, let x (n) is finite length sequence (4, 5, 3, 1) and h (n) equal to finite length sequence (2, 7, 9, 3). The linear convolution of x (n) and h (n) can be solved by several methods, resulting in the sequence Y (n) = (8, 38, 77, 80, 49, 18, 3). Performing convolution using graphical method or formula based method is easy but it is quite lengthy and takes more time for calculation, again it is difficult to implement therefore among all the method given by john pierra easy to compute and implement, it is set up like conventional multiplication. Where the convolution of x(n) and h(n) is as shown in fig1. As shown in the fig1 calculation of convolution sum is very easy using john perra method, it is like performing multiplication except the carry is not propagated out the column.

#### **IV. DECONVOLUTION METHOD**

Deconvolution is an operation which takes two functions one input is convolved sequence y(n) where as other inputis h(n), and produces a single function output x(n). For Deconvolution a direct method is presented for performing Deconvolution of two finite length sequences. This method is similar to performing long division and polynomial division. The basic recursive Deconvoltion method is used for finding Deconvoltion of finite length sequences. The recursion method works similar to performing long division [10]. To illustrate the method further Consider the example 2, let Y(n) be the convolved sequence equal to

(8,38,77,80,49,18,3) and h(n) be the finite length sequence equal to (2,7,9,3). Performing Deconvolution resulting X (n) = (4,5,3,1). The Deconvolution of finite length sequences Y (n) and h (n) using recursion method as shown below Fig.2.

				4	5	3	1	-		(n)
2	7	9	3	8	38	77	80	49	18	3
				8	28	36	12			
				0	10	41	68	49	18	3
					10	35	45	15		
				0	6	23	34	18	3	
					1.546.946	6	21	27	9	3
						0	2	7	9	3
							2	7	9	3
				1			0	0	0	0

Fig.2. Deconvolution by Recursion Method.

(1)



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#### **V. VEDIC MULTIPLIER**

In this paper a systematic Vedic multiplier using UrdhavaTiryagbhyam sutra is used for multiplication. Among all multiplier this Vedic multiplier performs faster multiplication and occupies less area. In the proposed convolution method the Multiplier is based on UrdhavaTiryagbhyam(vertically and crosswise).Vedic mathematics provides easiest way to perform multiplication. It reduces the typical calculation which is difficult to compute using conventional multiplier. UrdhavaTiryagbhyam is general multiplication formula applicable for all types of

Y. using the Vedic multiplication method consider 2 bit at a time and perform the multiplication on using 2 bit multiplier. The following Fig.3 shows the multiplication of  $4 \times 4$  numbers using Vedic multiplier.



Fig.3. Block Diagram presentation for 4 X 4 Multiplication.

Each block as shown above is 2 x 2 multiplier.  $X_3 X_2$  and  $Y_3 Y_2$  are given as input to first 2 x 2 multiplier.  $X_3 X_2$  and  $Y_1 Y_0$  is given as input to second block.  $X_1 X_0$  and  $Y_3 Y_2$  is given as input to the third block of multiplier.  $X_1 X_0$  and  $Y_1 Y_0$  is given as input to last block. The final result of multiplication is of 8 bit say  $M_7 M_6 M_5 M_4 M_3 M_2 M_1 M_0$ , calculated as given below.

$\begin{array}{c} X_3 \ X_2 \\ Y_3 \ Y_2 \end{array}$	$\begin{array}{c} X_3 \hspace{0.1cm} X_2 \\ Y_1 \hspace{0.1cm} Y_0 \end{array}$	$\begin{array}{c}X_1 & X_0 \\ Y_3 & Y_2\end{array}$	$\begin{array}{c} X_1 \hspace{0.1cm} X_0 \\ Y_1 \hspace{0.1cm} Y_0 \end{array}$
$M_{33}M_{32}M_{31}M_{30}$	M <sub>23</sub> M <sub>22</sub> M <sub>21</sub> M <sub>20</sub>	M <sub>13</sub> M <sub>12</sub> M <sub>11</sub> M <sub>10</sub>	M <sub>03</sub> M <sub>02</sub> M <sub>01</sub> M <sub>00</sub>

Assuming the output of each multiplication is as given above. For the final result, the multiplication result of each 2x2 multiplier block is arranged in specific manner as shown

multiplication. The parallelism in generation of partial product improves the speed of multiplication. For computing big multiplication of N X N, the number is divided in to small blocks and utilize for design. For higher number of bit some modification is required. Divide the number in to two equal parts. Let's analyse 4 x 4multiplications, Say  $X_3X_2X_1X_0$  and  $Y_3 Y_2 Y_1 Y_0$ . The result of multiplication of these two numbers is given by  $M_7 M_6 M_5M_4 M_3 M_2 M_1 M_0$ . Let's divide the X and Y in to two parts say  $X_3 X_2$  and  $X_1 X_0$  for X and  $Y_3 Y_2$  and  $Y_1 Y_0$  for

below. Add the middle product term along with the term shown below.

The first two outputs  $M_0$  and  $M_1$  are same as that of  $M_{00}$  and  $M_{01}$ .one 4bit full adder is used to add the ( $M_{23}$   $M_{22}$   $M_{21}M_{20}$ ) and ( $M_{13}$   $M_{12}$   $M_{11}$   $M_{10}$ ). The result of addition of first adder is added with the ( $M_{31}$   $M_{32}$   $M_{03}$   $M_{02}$ ). The result of addition of second full adder gives  $M_5$   $M_4$   $M_3$   $M_2$  bit of final multiplication. The carry generated during first full adder operation is added using half adder with carry generated during second full adder operation. The final sum and carry of half adder is added with  $M_{33}$   $M_{32}$  gives  $M_7$   $M_6$  bit of final multiplication result. The same method can be extended for 8, 16, 32 input bits.

#### **V. VEDIC DIVIDER**

In this paper a systematic method is used for division which based on Paravartya Sutra. Paravartya Sutra help to minimize computation and maintain accuracy even as the number of iteration is reduced. It provides easier and logically simple implementation. According to paravartya sutra, all the digit of the divisor is complemented except the most significant digit. This complemented digit is initially multiplied with the most significant digit of the dividend and this multiplication result is added with columns of dividend. The result of addition is again multiplied with complemented digits of Divisor and added with the remaining column of the dividend, followed successive multiplication and addition of consecutive column. The summation of all columns results forms quotient and remainder. Implementation of the algorithm is illustrated using an example. Assume the



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dividend is 14589 and divisor is 132. The division of this two numbers using paravartya sutra is shown in fig.4.

	Diviso	or			Divid	lend	
1	3	2	1	4	5	8	9
	-3	-2		-3	-2		
			Č.		-3	-2	
			6			0	0
			1	1	0	6	9
			Quo	tient =	110	Reminde	er = 69

Fig.4. Division using paravartya sutra.

#### VI. SIMULATION AND RESULT

Simulation and results of this paper is as shown in bellow Figs. 5 to 7.



Fig.6. RTL schematic.

**TABLE I: Design Summary** 

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slice LUTs	880	<mark>6</mark> 3400		1%
Number of fully used LUT-FF pairs	0	880		0%
Number of bonded IOBs	112	210		53%



Fig.5. Block Diagram.

Name	Value 0	ns  100 ns	200 ns 100 ns
Korv0[7	00000000	00001100	00000000
Conv1[8	000001100	000100001	000001100
Conv2[9	0000010001	0000101001	0000010001
▶ 🙀 corw3[9	0000100101	0000110000	0000100101
▶ 🍓 conv4[9	0000100010	0000100010	0000100010
conv5[8	000011100	000001000	000011100
conv6(7	00010000	00000000	00010000
▶ 🌠 d0(3:0]	0100	0000	0100
d1[3:0]	0010	0010	0010
▶ 📢 d2[3:0]	0011	0110	0011
▶ 📢 d3[3:0]	0000	0011 X	0000
▶ 📷 a[3:0]	0100		0100
▶ 📢 b[3:0]	0101		0101
▶ 📑 c[3:0]	0011		0011
▶ 📢 d[3:0]	0100		0100
▶ 📢 e[3:0]	0100	0000	0100
▶ 📢 f[3:0]	0010		0010
▶ 📢 g[3:0]	0011	0110	0011
M h(3:01	0000	0011	0000

Fig.7.Output waveform.

#### VII. CONCLUSION

The main focus of this paper is to introduce a method for calculating the linear convolution, circular convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform. The execution time and area of the proposed method for convolution using vedic multiplication algorithm is compared with that of convolution with the simple multiplication is less. An extension of the proposed linear convolution approach circular convolution using vedic multiplier is also introduced which has less delay and area than the conventional method. This paper also introduced a straightforward approach to performing the decon volution.



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#### VIII. REFERENCES

[1] J. G. Proakis and D. G. Manolakis, "Digital Signal Processing: Principles, Algorithm, and Applications," 2nd Edition. New York Macmillan, 1992.

[2] Pierre, John W. "A novel method for calculating the convolution sumof two finite length sequences." Education, IEEE Transactions on 39.1(1996): 77-80.

[3] Rudagi, J. M., VishwanathAmbli, VishwanathMunavalli, RavindraPatil, and VinaykumarSajjan. "Design and implementation of efficient multiplier using Vedic mathematics." (2011): 162-166.

[4] Vaidya, Sumit, and Deepak Dandekar. "Delay-Power Performance Comparison of multipliers in VLSI circuit design." International Journal of Computer Networks & Communications (IJCNC) 2.4 (2010): 47-56. [5] Akhter, Shamim. "VHDL implementation of fast NxN multiplier basedonvedic mathematic." In Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on, pp. 472-475. IEEE, 2007. [6] Thapliyal, Himanshu, and M. B. Srinivas. "High Speed Efficient NxNBitParallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics." Enformatika Trans 2 (2004): 225-228.

[7] Lomte, Rashmi K., and P. C. Bhaskar. "High Speed Convolution andDeconvolution Using UrdhvaTriyagbhyam." VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on. IEEE, 2011.

[8] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics." Motilalanarsidass, New Delhi, India, 1994.

[9] Hanumantharaju, M. C., et al. "A High Speed Block Convolution usingAncient Indian Vedic Mathematics." Conference on Computational Intelligence and Multimedia Applications, 2007. International Conferenceon. Vol. 2. IEEE, 2007.

[10] Itawadiya, Akhalesh K., et al. "Design a DSP operations using vedicmathematics." Communications and Signal

Processing (ICCSP), 2013International Conference on. IEEE, 2013.