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Compensation of AC and DC Loads of A Three-phase DSTATCOM By using A Fast-acting DC-link voltage Controller

R Chandrashekhar Reddy, M.Tech Student, PVKK Institute of Technology, Anantapur
D Mahesh Kumar, Head of the Department, PVKK Institute of Technology, Anantapur

Abstract

When adjusting rapidly fluctuating unbalanced and nonlinear loads, the transient responsiveness of the distribution static compensator (DSTATCOM) is critical. Any change in the load has a direct impact on the dc-link voltage. When the load is suddenly removed, the dc-link voltage rises above the reference value, but when the load is suddenly increased, the dc-link voltage falls below the reference value. Variation of the dc-link voltage within the permitted limits is required for successful DSTATCOM functioning. To keep the dc-link voltage at the reference value, a proportional-integer (PI) controller is often utilised. Its input is the difference between the capacitor voltage and its reference value. The standard PI dc-link voltage controller, on the other hand, has a delayed transient response. The energy of a dc-link capacitor is used to suggest a fast-acting dc-link voltage controller in this research. To achieve such quick transient reaction, mathematical formulae are presented to calculate the gains of the traditional controller based on fast-acting dc-link voltage controllers. To validate the proposed controller, thorough simulation and experimental investigations are conducted.

Index Terms—DC-link voltage controller, distribution static compensator (DSTATCOM), fast transient response, harmonics, load compensation, power factor, power quality (PQ), unbalance, voltage-source inverter (VSI).

INTRODUCTION

THE proliferation of power-electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power-quality (PQ) problems in the power distribution net- work. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion, high levels of neutral-to-ground voltage, and interference with communication systems [1], [2]. The literature records the evolution of different custom power devices to mitigate the above power-quality problems by injecting voltages/currents or
both into the system [3]–[6].

The shunt-connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is sup- ported by a dc storage capacitor with proper dc voltage across it.

One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature [7]–[11] to compute the reference compensator cur- rents. However, due to the simplicity in formulation and no con- fusion regarding the definition of powers, the control algorithm based on instantaneous symmetrical component theory [11] is preferred. Based on this algorithm, the compensator reference currents are given as follows:

$$(i^*_{fa}, i^*_{fb}, i^*_{fc}) = i_{la} - \begin{Bmatrix} \frac{v_{sa}+\gamma(v_{sb}-v_{sc})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \\ \frac{v_{sb}+\gamma(v_{sc}-v_{sa})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \\ \frac{v_{sc}+\gamma(v_{sa}-v_{sb})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \end{Bmatrix}$$

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(1)

where is the desired phase angle between the supply voltages and compensated source currents in the respec- tive phases. For unity power factor operation, ϕ 0, thus 0.
The term is the dc or average value of the load power. Theterm in (1) accounts for the losses in the VSI without any dc loads in its dc link. To generate $P_{\rm dc}$, a suitable closed-loop dc-link voltage controller should be used, which will regulate the dc voltage to the reference value.

For the DSTATCOM compensating unbalanced and non- linear loads, the transient performance of the compensator is decided by the computation time of average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of the average load power. Therefore, the transient performance of the compensator mostly depends on the computation of $P_{\rm lavg}$. In this paper, $P_{\rm lavg}$ is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics presence in voltages and currents. Although the computation of $P_{\rm dc}$ is generally slow and updated once or twice in a cycle, being a small value compared to $P_{\rm lavg}$, it does not play a significant role in transient performance of the compensator.

In some of the electric power consumers, such as the telecom-
munications industry, power-electronics drive applications, etc., there is a requirement for ac as well as dc loads [12]–[15]. The telecommunication industry uses several parallel-connected

switch-mode rectifiers to support dc bus voltage. Such an arrangement draws nonlinear load currents from the utility. This causes poor power factor and, hence, more losses and less efficiency. Clearly, there are PQ issues, such as unbalance, poor power factor, and harmonics produced by telecom equipment in power distribution networks. Therefore, the functionalities of the conventional DSTATCOM should be increased to mitigate the aforementioned PQ problems and to supply the dc loads from its dc link as well. The load sharing by the ac and dc bus depends upon the design and the rating of the VSI. This DSTATCOM differs from conventional one in the sense that its dc link not only supports instantaneous compensation but also supplies dc loads.

However, when the dc link of the DSTATCOM supplies the dc load as well, the corresponding dc power is comparable to the average load power and, hence, plays a major role in the transient response of the compensator. Hence, there are two important issues. The first one is the regulation of the dc-link voltage within prescribed limits under transient load conditions. The second one is the settling time of the dc–link voltage controller. Conventionally, a PI controller is used to maintain the dc-link voltage. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional dc-link voltage controllers is slow, especially in applications where the load changes rapidly. Some work related to dc-link voltage controllers and their stability is reported in [16]–[20]. However, the work is limited to rectifier units where switching patterns are well defined and analysis can be easily carried out. In this paper, a fast-acting dc-link voltage controller based on the dc-link capacitor energy is proposed. The detailed modeling, simulation, and experimental verifications are given to prove the efficacy of this fast-acting dc-link voltage controller. There is no systematic procedure to design the gains of the conventional PI controller used to regulate the dc-link voltage of the DSTATCOM. Herewith, mathematical equations are given to design the gains of the conventional controller based on the fast-acting dc-link voltage controllers to achieve similar fast transient response.

I. DSTATCOM FOR COMPENSATING AC AND DC LOADS

Various VSI topologies are described in the literature for realizing DSTATCOM to compensate unbalanced and nonlinear loads [21]–[29]. Due to the simplicity, the absence of unbalance in the dc-link voltage and independent current tracking with respect to other phases, a three-phase H-bridge VSI topology is chosen. Fig. 1 shows a three-phase, four-wire-compensated system using an H-bridge VSI topology-based DSTATCOM compensating unbalanced and nonlinear ac load. In addition to this, a dc load is connected across the dc link. The DSTATCOM consists of 12 insulated-gate biploar transistor (IGBT) switches each with an antiparallel diode, dc storage capacitor, three isolation transformers, and three interface inductors. The star point of the isolation transformers (n') is connected to the neutral of load and source . The

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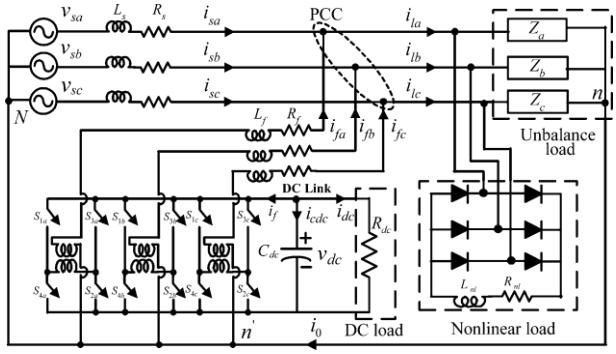

Fig. 1. Three-phase, four-wire compensated system using the H-bridge VSI topology-based DSTATCOM.

H-bridge VSIs are connected to the PCC through interface inductors. The isolation transformers prevent a short circuit of the dc capacitor for various combinations of the switching states of the VSI. The inductance and resistance of the iso- lation transformers are also included in L_f and R_f. The source voltages are assumed to be balanced and sinusoidal. With the supply being considered as a stiff source, the feeder impedance (L_s- R_s) shown in Fig. 1 is negligible and, hence, it is not accounted in state-space modeling. To track the desired compensator currents, the VSIs operate under the hysteresis band current control mode due to their simplicity, fast re- sponse, and being independent of the load parameters [30]. The DSTATCOM injects currents into the PCC in such a way as to cancel unbalance and harmonics in the load currents. The VSI operation is supported by the dc storage capacitor $C_{\rm dc}$ with voltage across it. The dc bus voltage has two functions, that is, to support the compensator operation and to supply dc load. While compensating, the DSTATCOM maintains the balanced sinusoidal source currents with unity power factor and supplies the dc load through its dc bus.

II. State-Space Model of the DSTATCOM

For the DSTATCOM topology shown in Fig. 1, the pairs of switches S_{1a}- S_{2a} and S_{4a}- S_{3a} are always ON and OFF in compli-mentary mode. The ON and OFF states of these switches are rep- resented by a binary logic variable S_a and its complement . Thus, when switches S_{1a} - S_{2a} are ON, it implies that switches S_{4a}- S_{3a} are OFF. This is represented by ,and vice versa. In a similar way, and represent gating signals for switches S_{1b}- - - - S_{3c}, respectively. Using these notations for the system shown in Fig.1, the state-space equations are written as follows:

$$\dot{x} = Ax + Bu \qquad (2)$$

where state vector $x$and input vector $u$are given by

$$x = [i_{fa} \quad i_{fb} \quad i_{fc} \quad v_{\rm dc}]^{\Gamma} \qquad (3)$$

$$u = [v_{sa} \quad v_{sb} \quad v_{sc}]^{\Gamma} \qquad (4)$$

$v_{\rm dc}$

$\bar{S}_a$

$S_a = 1, \bar{S}_a = 0$

$S_b, \bar{S}_b, S_c \quad \bar{S}_c$

$S_{2b}, S_{4b}\ S_{3b}, S_{1c}\ S_{2c}, S_{4c}$

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$$u_c = K_p\,(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}}) + K_i \int (V_{\mathrm{dcref}} - v_{\mathrm{dc}})\mathrm{dt} + K_d\, d(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}})/\mathrm{dt}. \quad (7)$$

where the superscript Γ stands for the transpose operator.

System matrix (A) and input matrix (B) are given as follows:

$$A = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & \frac{(S_a-\bar{S}_a)}{L_f} \\ 0 & -\frac{R_f}{L_f} & \frac{(S_b-\bar{S}_b)}{L_f} \\ -\frac{(S_a-\bar{S}_a)}{C_{\mathrm{dc}}} & -\frac{(S_b-\bar{S}_b)}{C_{\mathrm{dc}}} & -\frac{(S_c-\bar{S}_c)}{C_{\mathrm{dc}}} \end{bmatrix} \quad (5)$$

$$B = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \\ 0 & 0 \end{bmatrix}. \quad (6)$$

Using the above state-space model, the system state variables (x) are computed at every instant.

III. DC-Link Voltage Controllers

As mentioned before, the source supplies an unbalanced nonlinear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in Fig. 1. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc-link voltage, closed-loop controllers are used. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as

In (7), K_p, K_i, and K_d are proportional, integral, and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain K_p reduces rise time and steady-state error but increases the overshoot and settling time. An increase in integral gain K_i reduces steady-state error but increases overshoot and settling time. Increasing derivative gain K_d will lead to improved stability. However, practitioners have often found that the derivative term can behave against anticipatory action in case of transport delay. A cumbersome trial-and-error method to tune its parameters made many practitioners switch off or even exclude the derivative term [31], [32]. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following subsections.

A. Conventional DC-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in Fig. 2. To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the dif- ference between the actual and reference voltages. The power required by the capacitor can be expressed as follows:

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$$P_{\mathrm{dc}} = K_p(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}}) + K_i \int (V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}})\mathrm{dt}. \quad (8)$$

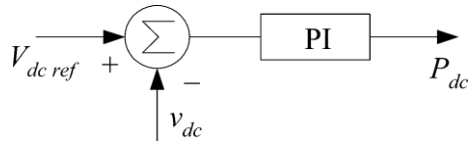

Fig. 2. Schematic diagram of the conventional dc-link voltage controller.

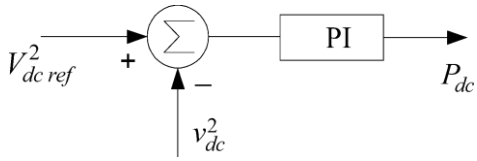

Fig. 3. Schematic diagram of the fast-acting dc-link voltage controller.

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase-a supply voltage. The sampling can also be performed at a quarter cycle depending upon the symmetry of the dc-link voltage waveform. The drawback of this conventional controller is that its transient response is slow, especially for fast-changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and, hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of K_p and K_i when P_{dc} is comparable to P_{lavg}.

B. Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc-link capacitor (W_{dc}) to charge from actual voltage (v_{dc}) to the reference value $(V_{\mathrm{dc\,ref}})$ can be computed as

$$W_{\mathrm{dc}} = \frac{1}{2} C_{\mathrm{dc}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) \quad (9)$$

In general, the dc-link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc power (P'_{dc}) required by the dc-link capacitor is given as

$$P'_{\mathrm{dc}} = \frac{W_{\mathrm{dc}}}{T_c} = \frac{1}{2T_c} C_{\mathrm{dc}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) \quad (10)$$

where T_c is the ripple period of the dc-link capacitor voltage. Some control schemes have been reported in [33] and [34]. However, due to the lack of integral term, there is a steady-state error while compensating the combined ac and dc loads. This is eliminated by including an integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages. This controller is shown in Fig. 3 and the total dc power required by the dc-link capacitor is computed as follows:

$$P_{\mathrm{dc}} = K_{\mathrm{pe}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) + K_{\mathrm{ie}} \int \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) \mathrm{dt}. \quad (11)$$

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The coefficients $K_{\rm pe}$ and $K_{\rm ie}$ are the proportional and integral gains of the proposed energy-based dc-link voltage controller.

As an energy-based controller, it gives fast response compared to the conventional PI controller. Thus, it can be called a fast-acting dc-link voltage controller. The ease in the calculation of the proportional and integral gains is an additional advantage. The value of the proportional controller gain $K_{\rm pe}$ can be given as

$$K_{\rm pe} = \frac{C_{\rm dc}}{2T_c}. \tag{12}$$

For example, if the value of dc-link capacitor is 2200 μF and the capacitor voltage ripple period as 0.01 s, then $K_{\rm pe}$ is computed as 0.11 by using (12). The selection of $K_{\rm ie}$ depends upon the tradeoff between the transient response and overshoot in the compensated source current. Once this proportional gain is selected, integral gain is tuned around and chosen to be 0.5. It is found that if $K_{\rm ie}$ is greater than $K_{\rm pe}/2$, the response tends to be oscillatory and if $K_{\rm ie}$ is less than $K_{\rm pe}/2$, then response tends to be sluggish. Hence, $K_{\rm ie}$ is chosen to be $K_{\rm pe}/2$.

IV. Design of Conventional Controller Based onthe Fast-Acting DC-Link Voltage Controller

The conventional dc-link voltage controller can be designed based on equations given for the fast-acting dc-link voltage controller as in (11) and can be written as

$$P_{\rm dc} = K_{\rm pc}(V_{\rm dc\,ref} + v_{\rm dc})(V_{\rm dc\,ref} - v_{\rm dc}) + K_{\rm ie}\int (V_{\rm dc\,ref} + v_{\rm dc})(V_{\rm dc\,ref} - v_{\rm dc})\mathrm{dt}. \tag{13}$$

It can be also written as

$$P_{\rm dc} = K_p'(V_{\rm dc\,ref} - v_{\rm dc}) + K_i'\int (V_{\rm dc\,ref} - v_{\rm dc})\mathrm{dt} \tag{14}$$

where

$$K_p' = K_{\rm pc}(V_{\rm dc\,ref} + v_{\rm dc}) \tag{15}$$

$$K_i' = K_{\rm ic}(V_{\rm dc\,ref} + v_{\rm dc}). \tag{16}$$

It is observed from the aforementioned equations that the gains of proportional and integral controllers vary with respect to time. However, for small ripples in the dc-link voltage, $v_{\rm dc} \approx V_{\rm dc\,ref}$, therefore, we can approximate the above gains to the following:

$$K_p' \approx 2K_{\rm pc}V_{\rm dc\,ref}$$

$$K_i' \approx 2K_{\rm ic}V_{\rm dc\,ref}.$$

$$\frac{V_{\rm dc\,ref} + v_{\rm dc}}{2V_{\rm dc\,ref}} \qquad \frac{}{v_{\rm dc}}$$

TABLE I
Simulation Parameters

System Parameters	Values
supply voltage	400 V (L-L), 50 Hz
Unbalanced load	Z_a = 25 Ω, Z_b = 44 + j25.5 Ω and Z_c = 50 + j86.6 Ω
Nonlinear load	Three-phase full wave rectifier drawing a dc current of 5 A
DC load	R_{dc} = 100 Ω
DC capacitor	C_{dc} = 2000 µF
Interface inductor	L_f = 26 mH, R_f = 0.25 Ω
Reference dc link voltage	$V_{dc\,ref}$ = 520 V
Hysteresis band	±h = 1.0 A
Gains of conventional dc link voltage controller	K_p = 40, K_i = 20
Gains of fast acting dc link voltage controller	K_p = 0.11, K_i = 0.055

where $E_{er} = V_{\rm dc\,ref}^2 - v_{\rm dc}^2$ and

$$\frac{P_{\rm dc}}{E_r} = \frac{K_p'(s + K_i'/K_p')}{s} \tag{20}$$

where $E_r = V_{\rm dc\,ref} - v_{\rm dc}$. Since K_i'/K_p' is the same as $K_{\rm ic}/K_{\rm pc}$, the higher gain in the conventional PI controller renders less stability than that of the proposed energy-based dc-link controller. For nearly the same performance, the conventional PI controller has gains which are 364 (40/0.11 from Table I) times larger than that of that proposed one. Also, the amplifier units used to realize these gains need more design considerations and are likely to saturate when used with higher gains.

V. Selection of the DC-Link Capacitor

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in Fig. 1 is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by $X \times 1000$ J/s. Let us further assume that the compensator deals with half (i.e., $X/2$) and twice (i.e.,

(17)

(18)

The relations (17)–(18) give approximate gains for a conven-

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tional PI controller. This is due to the fact that is not really equal to until variation in is small during transients. Hence, the designed conventional PI controller works only on approximation. The open-loop gains for the two cases are given by

$$\frac{P_{\rm dc}}{E_{er}} = \frac{K_{\rm pc}(s + K_{\rm ic}/K_{\rm pc})}{s} \tag{19}$$

$2X$) capacity under the transient conditions for n cycles with the system voltage period of Ts. Then, the change in energy to be dealt with by the dc capacitor is given as

$$\Delta E = (2X - X/2)nT. \tag{21}$$

Now this change in energy (21) should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-link voltage from 1.4 V_m to 1.8 V_m during the transient conditions where V_m is the peak value of phase voltage. Hence, we can write

$$\frac{1}{2}C_{\rm dc}[(1.8\,{\rm V}_m)^2 - (1.4\,{\rm V}_m)^2] = (2X - X/2)nT \tag{22}$$

which implies that

$$C_{\rm dc} = \frac{3XnT}{(1.8\,{\rm V}_m)^2 - (1.4\,{\rm V}_m)^2}. \tag{23}$$

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For example, consider a 10-kVA system (i.e., VA_r=10 kVA), system peak voltage V_m = 325.2 V, m = 0.5, and T = 0.02 s. The value of C_{dc} computed using (23) is 2216 μF. Practically, 2000 μF is readily available and the same value has been taken for simulation and experimental studies.

VI. Simulation Studies

The load compensator with H-bridge VSI topology as shown in Fig. 1 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the PCC. The ac load consists of a three-phase unbalanced load and a three-phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance (R_{dc}) as shown in the figure. The dc load forms 50% of the total power requirement. The system and compensator parameters are given in Table I.

By monitoring the load currents and PCC voltages, the average load power is computed. At every zero crossing of phase a voltage, P_{dc} is generated by using the dc-link voltage controller. The state-space equations are solved to compute the actual compensator currents and dc-link voltage. These actual currents are compared with the reference currents given by (1) using hysteresis current control. Based on the comparison, switching signals are generated to compute the actual state variables by solving the state-space model given in (2). The source voltages and load currents are plotted in Fig. 4(a) and (b). The load currents have total harmonic distortions of 8.9%, 14.3%, and 21.5% in phases $a, b,$ and c, respectively. The unbalance in load currents results in neutral current as illustrated in the figure.

The compensator currents and compensated source currents are shown in Fig. 4(c) and (d). As seen from Fig. 4(d), the source currents are balanced sinusoids; however, the switching frequency components are superimposed over the reference currents due to the switching action of the VSI. The currents have a unity power factor relationship with the voltages in the respective phases. The THDs in these currents are 3.6%, 3.7%, and 3.9% in phases $a, b,$ and c, respectively. There are notches in the source currents due to finite bandwidth of the VSI.

The transient performance of the conventional and fast-acting dc-link voltage controllers are studied by making sudden changes in the ac load supplied by the ac load bus as well as the dc load supplied by the dc link. In the simulation study, the load is halved at the instant t =0.4 s and brought back to full load at t=0.8 s. The transient performance is explained in the following subsections.

A. *Transient Performance of Conventional DC-Link Voltage Controller*

The conventional dc-link voltage controller as given in (8) is used to generate the dc load power P_{dc} which is inclusive of losses in the inverter. The transient performance of the compensator is shown in Fig. 5(a) and (b). The total load, which is a combination of linear unbalanced and nonlinear load (as given in Table I), is halved at the instant 0.4 s. Due to a sudden reduction in the load, the dc-link capacitor absorbs surplus power from the source. Therefore, there is an increase in dc-link capacitor voltage above the reference value. Based on the values

t =

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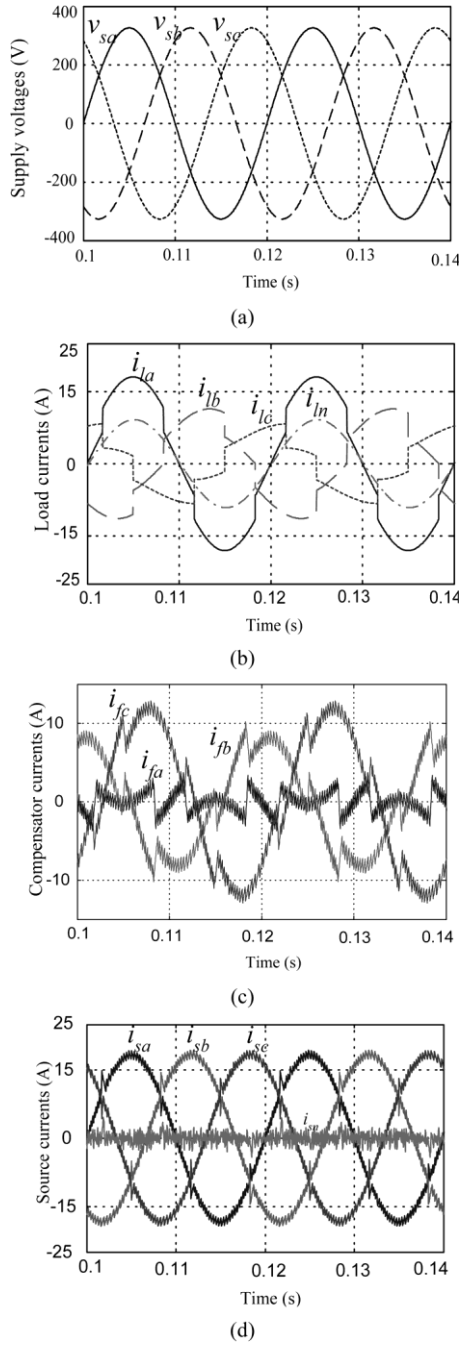

Fig. 4. (a) Supply voltages. (b) Load currents. (c) Compensator currents. (d) Compensated source currents.

of PI controller gains, the dc-link capacitor voltage controller will be brought back to the reference value after a few cycles.

Similarly, when the load is switched back to the full load at instant 0.8 s, the dc capacitor supplies power to the load momentarily and, hence, the dc-link voltage falls below the refer- ence value. Due to the PI controller action, the capacitor voltage will gradually build up and reach its reference value. If gains of the conventional dc-link voltage controller are not properly chosen, the dc-link voltage would have undesirable overshoot and considerably large settling time. Consequently, the perfor- mance of the load connected to the dc link also gets affected due to the above factors. It can be observed from Fig. 5(a) and (b)

$t =$

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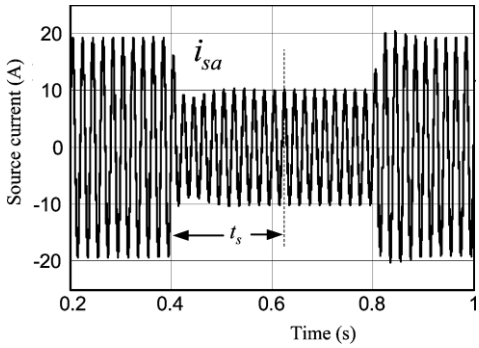
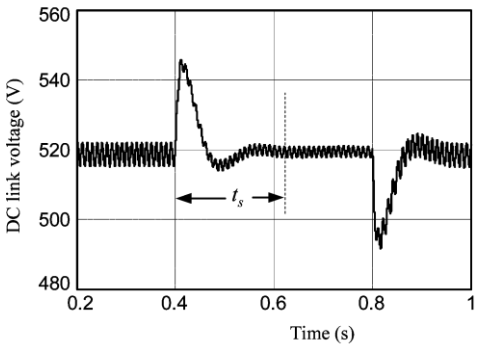


(a)



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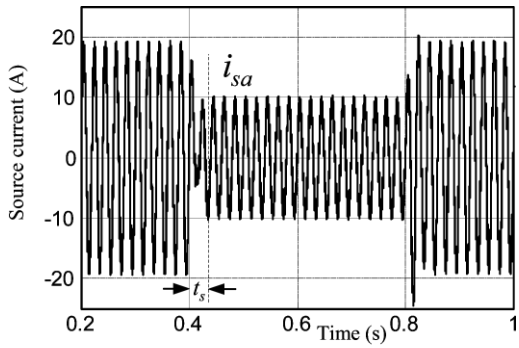
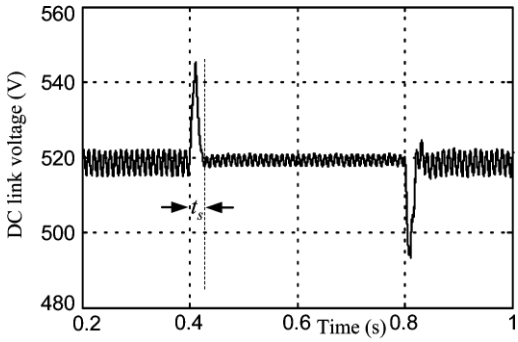


(a)



(b)

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Fig. 5. Transient response of the conventional controller. (a) Compensated source current in phase . (b) DC-link voltage.

that the conventional dc-link voltage controller takes about a ten cycle period to reach the reference voltage during load transient. This is indicated by time duration t_s in these figures.

B. Transient Performance of Fast-Acting DC-Link VoltageController

The dc load power P_{dc} is computed by using the fast-acting dc-link voltage controller as given in (11). Transients in the load are considered the same as in the above simulation study. Fig. 6(a) and (b) illustrates the phase source current and dc-link capacitor voltage during the load transients.

At the instant t = 0.4 s, the capacitor voltage increases due to the sudden removal of the load. The fast-acting dc-link voltage controller takes action at the instant 0.41 s. This is because the controller output is updated at every half cycle. It computes the dc load power P_{dc} needed to bring the capacitor voltage to the reference value in a half cycle. Therefore, the dc-link voltage reaches its reference voltage at the instant 0.42 s. When the dc-link voltage is more than the reference value, P_{dc} is less. Therefore, the source currents are less in magnitude.

At the instant 0.8 s, the dc-link voltage falls below the reference voltage due to a sudden increase in load. As explained earlier, the fast-acting controller brings the dc-link voltage to its reference value at 0.82 s with almost the same rise in voltage as that of the conventional dc-link voltage controller. A close observation of the figure would reveal that the fast-acting dc-link voltage controller can regulate the capacitor voltage within a half cycle period which is indicated by t_s. Owing to its good transient performance, it is preferred over the conven-tional dc-link voltage controller.

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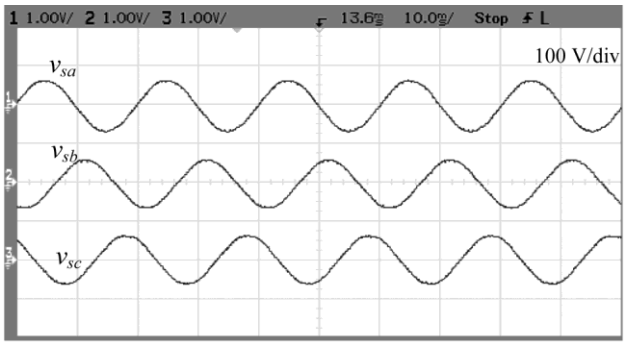
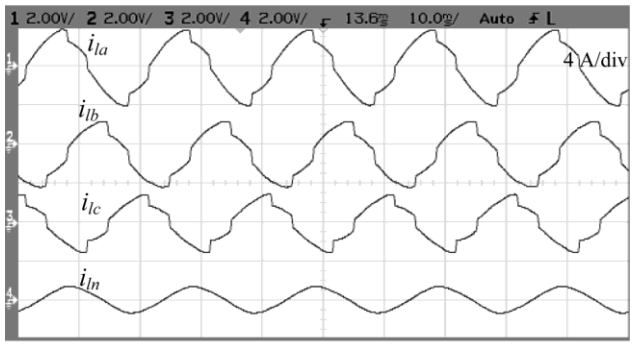
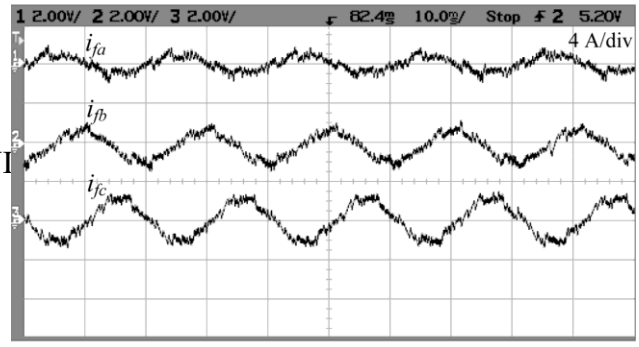
Fig. 6. Transient response of the fast-acting controller. (a) Compensated sourcecurrent in phase . (b) DC-link voltage.



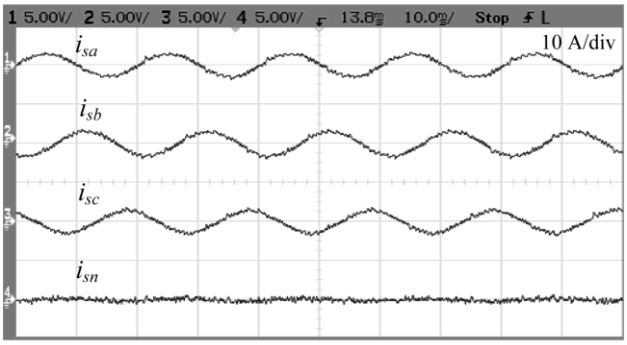
(a)



(b)



(c)



(d)

VI

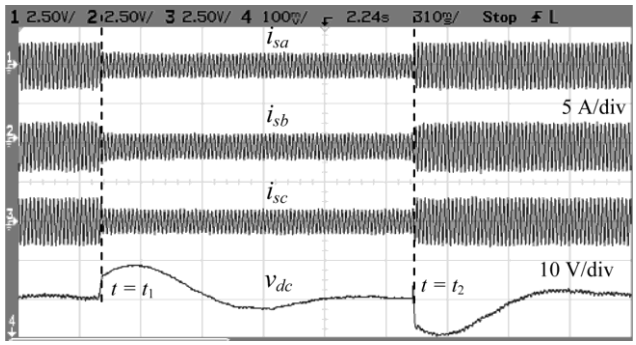


Fig. 9. Source currents and dc-link voltage with a conventional dc-link voltage controller.

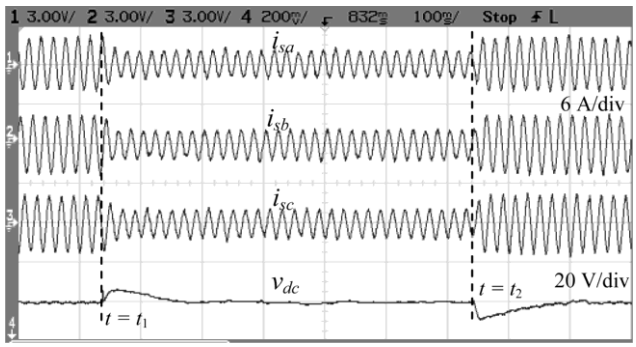


Fig. 10. Source currents and dc-link voltage with a fast-acting dc-link voltage controller.

CONCLUSION

A VSI topology for DSTATCOM compensating ac unbalanced and nonlinear loads and a dc load supplied by the dc link of the compensator is presented. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. An energy-based fast-acting dc-link voltage controller is suggested to ensure the fast transient response of the compensator. Mathematical equations are developed to compute the gains of this controller. The efficacy of the proposed controller over the conventional dc-link voltage controller is established through the digital simulation and experimental studies. It is observed from these studies that the proposed dc-link voltage controller gives fast transient response under load transients.

REFERENCES

[1] M. H. J. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. New York: IEEE Press, 2017.

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Fig. 8. (a) Supply voltages. (b) Load currents. (c) Compensator currents. (d) Source currents after compensation.

same. This is due to the use of the mechanical switch for the change of load, which cannot connect/disconnect the load in all three phases simultaneously at the instants t_1 and t_2, and due to other nonidealities in the system.

[2] W. M. Grady and S. Santoso*, Proc. IEEE Power Eng. Rev. Understanding Power System Harmonics, vol. 21, no. 11, pp. 8–11, 2017.*
[3] N. Hingorani, "Introducing custom power," *IEEE Spectr.*, vol. 32, no. 6, pp. 41–48, Jun. 2015.
[4] A. Ghosh and G. Ledwich*, Power Quality Enhancement Using Custom Power Devices. Norwell, MA: Kluwer, 2016*
[5] V. Dinavahi, R. Iravani, and R. Bonert, "Design of a real-time digital simulator for a D-STATCOM system," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1001–1008, Oct. 2014.
[6] D. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "A novel technique to compensate voltage sags in multiline distribution system and the interline dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1603–1611, Oct. 2016.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

[7] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625–630, May 2008.

[8] H. Kim, F. Blaabjerg, B. B. Jensen, and J. Choi, "Instantaneous power compensation in three-phase systems by using p-q-r theory," *IEEE Trans. Power Electron., vol. 17, no. 5, pp. 701–709, Sep. 2012.*

[9] F. Z. Peng and J. S. Lai, "Generalized instantaneous reactive power theory for three-phase power systems," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 1, pp. 293–297, Feb. 2006.

[10] T. Furuhashi, S. Okuma, and Y. Uchikawa, "A study on the theory of instantaneous reactive power," *IEEE Trans. Ind. Electron.*, vol. 37, no. 1, pp. 86–90, Feb. 2000.

[11] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," *IEEE Trans. Power Del.*, vol. 15, no. 1, pp. 417–422, Jan. 2000.

[12] S. Kim, M. H. Todorovic, and P. N. Enjeti, "Three-phase active harmonic rectifier (AHR) to improve utility input current THD in telecommunication power distribution system," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1414–1421, Sep./Oct. 2003.

[13] R. Redl and A. S. Kislovski, "Telecom power supplies and power quality," in *Proc. 17th Int. Telecommunications Energy Conf.*, Denmark, Oct. 29–Nov. 1 1995, pp. 13–21.

[14] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications—An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[15] A. S. Kislovski, "Telecom power-supply plants using three-phase rectifiers and active filters," in *Proc. 2nd Int. Telecommunications Energy Special Conf.*, Budapest, Hungary, Apr. 22–24, 1997, pp. 127–134.

[16] P. Verdelho and G. D. Marques, "DC voltage control and stability analysis of PWM-voltage-type reversible rectifiers," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 263–273, Apr. 1998.

[17] A. Prodic´ and G. D. Marques, "Compensator design and stability assessment for fast voltage loops of power factor correction rectifiers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1719–1730, Sep. 2007.

[18] D. Zhao and R. Ayyanar, "Space vector PWM with DC link voltage control and using sequences with active state division," in *Proc., IEEE Int. Symp. Industrial Electronics*, Montreal, QC, Canada, Jul. 9–12, 2006, vol. 2, pp. 1223–1228.

[19] K. Mahabir, G. Verghese, J. Thottuvelil, and A. Heyman, "Linear averaged and sampled data models for large signal control of high power factor AC-DC converters," in *Proc. 21st IEEE Power Electronics Specialists Conf.*, Jun. 1990, pp. 372–381.

[20] M. O. Eissa, S. B. Leeb, G. C. Verghese, and A. M. Stanković, "Fast controller for a unity power factor rectifier," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 1–6, Jan. 1996.

[21] M. K. Mishra, A. Ghosh, and A. Joshi, "A new STATCOM topology to compensate loads containing ac and dc components," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, Singapore, Jan. 23–27, 2000, vol. 4, pp. 2636–2641.

[22] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[23] M. Aredes, J. Häfner, and K. Heumann, "Three-phase four-wire shunt active filter control strategies," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 311–318, Mar. 1997.

[24] C. A. Quinn, N. Mohan, and H. Mehta, "Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single phase non-linear loads," in *Proc. Applied Power Electron. Conf.*, 1992, pp. 829–836.

[25] B. Singh, K. Al-Hadded, and A. Chandra, "A review of active filters for power quality improvements," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960–971, Oct. 1999.

[26] M. El-Habrouk, M. K. Darwish, and P. Mehta, "Active power filters: A review," *Proc. Inst. Elect. Eng., Electr. Power Appl.*, vol. 147, no. 5,pp. 403–413, Sep. 2000.

[27] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "An en- ergy-based control for an n-H-bridges multilevel active rectifier," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 670–678, Jun. 2005.

[28] S. Iyer, A. Ghosh, and A. Joshi, "Inverter topologies for DSTATCOM applications—A simulation study," *Elect. Power Syst. Res.*, vol. 75, pp. 161–170, Aug. 2005.

[29] B.-R. Lin and C.-H. Huang, "Implementation of a three-phase capac- itor-clamped active power filter under unbalanced condition," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1621–1630, Oct. 2006.

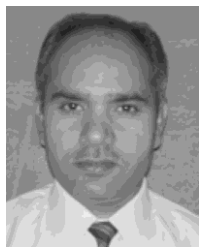
[30] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, Oct. 1998.

[31] K. H. Ang, G. Chong, and Y. Li, "PID control system analysis, design,and technology," *IEEE Trans. Control Syst. Technol.*, vol. 13, no. 4, pp.559–576, Jul. 2005.

[32] R. Ortega and R. Kelly, "PID self-tuners: Some theoretical and practical aspects," *IEEE Trans. Ind. Electron.*, vol. IE-31, no. 4, pp. 332–338, Nov. 1984.

[33] B. N. Singh, P. Rastgoufard, B. Singh, A. Chandra, and K. Al-Haddad,"Design, simulation and implementation of three pole/four-pole topologies for active filters," *Proc. Inst. Elect. Eng., Electr. Power Appl.*, vol. 151, no. 4, pp. 467–476, Jul. 2004.

[34] Y. Ye, M. Kazerani, and V. Quintana, "Modeling, control and imple- mentation of three-phase PWM converters," *IEEE Trans. Power Elec-tron.*, vol. 18, no. 3, pp. 857–864, May 2003.



Mahesh K. Mishra (S'00–M'02) received the B.Tech. degree in electrical engineering from the College of Technology, Patnagar, India, in 1991, the M.E. degree in electrical engineering from the University of Roorkee, Roorkee, India, in 1993, andthe Ph.D. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 2002.

He has about 16 years of teaching and research ex- perience. For about ten years, he was on the faculty of the Electrical Engineering Department, Visvesvaraya National Institute of Technology, Nagpur, India. Currently, he is a Professor in the Electrical Engineering Department, Indian Institute of Technology, Madras, India. His interests are in the areas of power distribution systems, power elec- tronics, and control systems.

K. Karthikeyan received the B.Eng. degree in elec- trical and electronics engineering from Syed Ammal Engineering College, Madurai Kamaraj University, Ramanathapuram, India, in 2002, the M.Eng. degreein power systems from the College of Engineering Guindy, Anna University, Chennai, India, in 2004, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Madras, Chennai,in 2007.

Currently, he is a Senior Engineer with Converteam EDC Private Ltd., Chennai. His fields of interest include power quality and power-electronics control in power systems.