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CONTROL OF DVR USING TURLY-NTD- PHASE LOCKED LOOP

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Abstract— The paper discusses how to use a DVR to resolve voltage related issues such as harmonics, sags, swells, and unbalance in supply voltages. The DVR is designed to address these concerns and offer a consistent power supply for sensitive loads. A strategy based on a really truly-non-frequency-dependent-transport-delay PLL (tNTD-PLL) is applied in evaluation of frequency, fundamental component and phase angle, which are then employed in a compensator to improve power quality by decreasing these values. The tNTD-PLL adds a delay element to the PLL's feedback loop, increasing transfer latency while decreasing double frequency oscillatory and offset errors. er than the targeted frequency. The control algorithm generates reference voltages, which are subsequently compared to the load voltages (sensed). The fault is subsequently fed into the PWM converter, which produces pulses for the DVR. It injects the voltages required to enhance the voltage-based issues related to power quality. The proposed DVR is simulated and designed using Simulink/MATLAB. A laboratory model of DVR with d-SPACE MicroLab-Box validates the simulation results.

Index Terms— Truly non-frequency-dependent transfer delay PLL, dynamic voltage restorer (DVR), sag, swell, harmonics, unbalance, optimization method.

I. INTRODUCTION

Widespread usage of Power electronic devices in power system causes various Voltage based power quality issues [1]. Bollen and Gu [2] explores the causes and consequences of these power quality concerns, offering information about how they harm sensitive electronic equipment's. Singh et al. [3] cover a wide range of challenges, including harmonics, voltage sags, and flicker, and provide practical methods for improving power quality. Zhan et al. [5] provide a three-dimensional voltage SV-PWM algorithm-based DVR. The authors provide a novel strategy to addressing power quality challenges, notably imbalanced and distorted loads [4]. Ghosh et al. designed a capacitor-supported DVR for distorted and unbalanced loads. Jurado et al. studied the neural network control in DVRs to improved control methods, which primes to the growth of adaptive power quality results [6]. Nielsen et al. investigate the various methods, giving helpful information for researchers and engineers working in DVR design and implementation [7]. Vilathgamuwa et al. [8] study the IDVR's technical specifications and ability to reduce voltage sags, providing valuable insights. Ho et al. examined voltage concerns and offered a control technique to increase DVR dynamic response [9]. Lam et al. studied and developed an effective strategy to decrease voltage fluctuations [10]. Saleh et al. [11] are interested in using wavelet transforms to detect and control voltage changes in real time. Roncero-Sanchez and Acha introduced a control mechanism for enhance DVR voltage rebuilding abilities. This study enhances multilevel converter-based DVRs and their use for enhancing power quality [12]. Babaei et al. studied

the use of direct converters to improve DVR performance in decreasing voltage fluctuations, and their findings shed light on the applications of this novel technology for improved power quality [13]. Ajaei et al. provided an effective and quick and control system for dynamic voltage restorers, with an emphasis on the creation of a control strategy that employs optimization approaches to improve DVR dynamic responsiveness and assure speedy and efficient compensation of voltage disturbances [14]. The IEEE 519-2014 Recommended Practices are a fundamental document that establishes the principles and standards for harmonic control in electric systems [15]. Jayaprakash et al. [16] investigate the control of a low-power DVR using a battery energy storage device. Chen et al. [17] present a novel approach for identifying synchronous phase-locked loops (SPLLs) and voltage sags that employs Les filters and an improved instantaneous symmetrical components method. Rauf and Khadkikar investigate the integration of solar systems with dynamic voltage restorers [18]. Carlos et al. [19] applies 02 dc-links and series converters to investigate dynamic voltage restorers for 3P 4SW systems. Mirjalili analyses the algorithm's application in optimization issues, demonstrating its efficiency in identifying solutions [20]. Biricik and Komurcugil [21] offer a sliding mode control approach designed for single-phase DVRs. Danbumrungtrakul et al. apply the zero active power tracking technique to assess the capability enhancement of dynamic voltage restorers [22]. Golestan et al. evaluate Kalman filter-based PLLs in steady-state and discuss their utility in power systems [23]. Li et al. offer a new voltage compensation philosophy for dynamic voltage restorers based on three-phase voltage elliptical parameters [24]. Pradhan and Mishra propose a p-q theory based DVR to improve PQ. [25]. Naidu et al. [26] describe a DVR using a quasi-newton strategy based on and optimized PI gains. Roldan-Perez et al. describe a sag detector based on delayed signal cancellation for a DVR in distorted grids. Their study addresses the difficulties of detecting voltage sags in non-ideal grid environments, yielding a unique approach for sag detection in dynamic voltage restorers [27]. Tu et al. perform a thorough analysis on using a DVR to nullify voltage [28] PQ issues, providing useful insights into DVRs increased capability for a broader spectrum of disturbances. Kandil and Ahmed look into the control and operation of a DVR with a self-supported dc bus [29]. Khergade et al. [30] investigate the impact of sag on power semiconductor drives and propose a mitigating strategy using an ESRF theory-based DVR. Akhtar and Saha [31] describe an NTD PLL with a simple technique for double-frequency oscillation rejection, as well as a unique PLL design for dynamic voltage restorers that improves performance by rejecting double-frequency oscillations. Biricik et al. [32] present a control method for DVRs based on a frequency-adaptive Brockett oscillator. Hasan et al. propose a new dual-slope-delta for a DVR based on a CSI, as well as a novel modulation technique for effective voltage sag reduction [33]. Bamigbade et al. [34] propose a FLL with a short single-phase transfer delay for use in power-systems. Shi et al. present a more efficient adaptive frequency-locked loop with a fixed transmission delay [35]. Du et al. [36] propose a supplementary approach for dynamic voltage restorers that improves microgrids' primary frequency responsiveness. The tNTD-PLL is extremely effective at reducing offset and double-frequency oscillatory errors, as well as noise, phase jitter, and frequency drift. By resolving these issues, tNTD-PLLs increase signal tracking accuracy and synchronization performance. Their one-of-a-kind design provides a strong solution for applications that

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require precise frequency control, improving stability against disturbances and assuring reliable operation in dynamic conditions. The NTD PLL's ability to efficiently reject undesirable oscillations makes it perfect for systems that require high precision and long-term stability in the face of changing conditions and noise.

II. System Arrangement and Principal of Operation

The diagram of tNTD-PLL DVR is shown in Fig 1. The DVR with distribution grid comprises of 3-Φ supply with source voltages ($v_{s(abc)}$), source impedance Zs (per phase), filtering inductors (L_f), R_f and C_f are the filtering resistance and capacitors, non-linear load is realized by L and R on the dc bus of six-pulse un-controlled rectifier, 3-leg IGBT VSC with self-supported dc capacitor (C_{dc}).

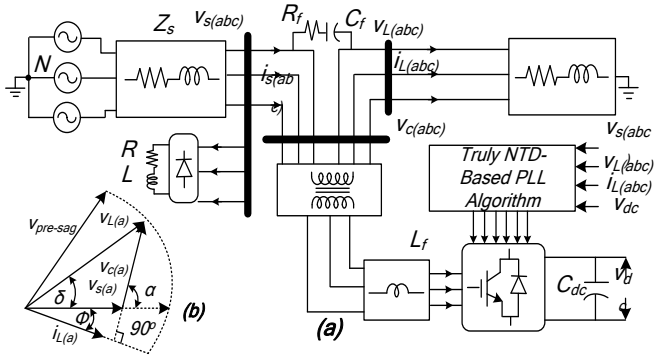

Fig. 1 Schematic diagram of NTD-PLL control algorithm

The dc bus voltage, currents (source), voltages (source), voltages of load and are sensed and given as input to truly NTD-PLL based control strategy. DVR is a widely adapted series device widely used to surmount the problems like harmonics in voltage, swell in voltage, sag in voltage and unbalance in source voltages in distribution grid.

During sag in grid (or source) voltages the VSC injects voltages in-phase with source to maintain the load voltages at 415V (rms). During swell in grid (or source) voltages the VSC injects voltages anti-phase with grid to maintain the load voltages at 415V (rms). During unbalance in grid voltages the VSC injects the voltage in unbalanced phase to grid to maintain a balanced load voltages and when the grid voltages contain harmonics than the DVR injects anti harmonics with the source to uphold the load voltages harmonic free. Filtering inductance L_f filters the DVR currents and R_f and L_f filters the ripples produced by VSC operation.

The proposed tNTD-PLL control strategy is used for production of fundamental voltages (load) is shown in Fig. 2 (a) and Fig. 2 (b).

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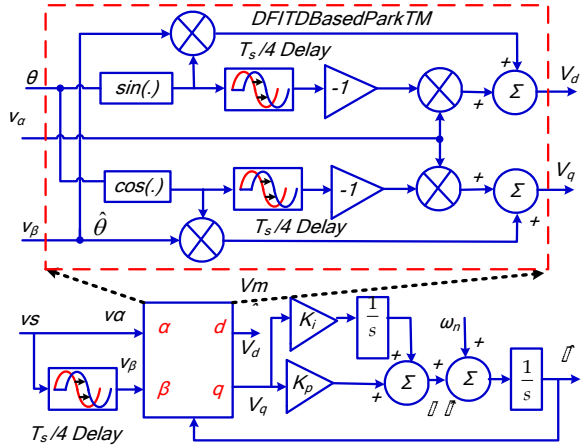

Fig. 2 (a) Block diagram of tNTD-PLL

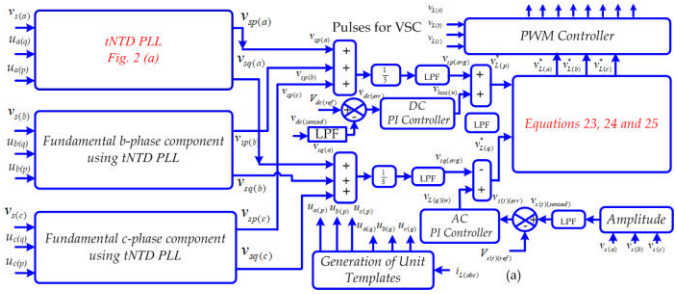

Fig. 2 (b) Schematic block diagram of the proposed tNTD-PLL

III. TRULY-NTD-PLL CONTROL ALGORITHM

The DVR performance banks on quick and accurate extraction of fundamental component source voltages. Fig. 2 (a) and (b) shows diagram of tNTD PLL and proposed control algorithm for DVR to extract reference voltages of load. Basic tNTD-PLL Block diagram shows V_s=source voltage, θ^=phase angle of V_s, terms angular frequency=ω, and estimated amplitude=V_m, respectively. Value of ω_n is the nominal frequency and k_i and k_p are the control variables.

A. Generation of Unit Templates

The three-phase source currents can be represented with 120^0 phase shift. The magnitude of currents can be calculated as [3]

$$i_t = \left[2/3(i_{s(a)}^2 + i_{s(b)}^2 + i_{s(c)}^2 \right]^{1/2} \quad (1)$$

where $i_{(m)}$ is the grid peak value (or source) current,

The unit templates (in-phase) of source currents are given as,

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$$u_{p(a)} = \frac{i_{s(a)}}{i_t}; u_{p(b)} = \frac{i_{s(b)}}{i_t}$$
$$u_{p(c)} = \frac{i_{s(c)}}{i_t} \quad (2)$$

The quadrature-phase components of unit templates are generated using the following [3]

$$w_{q(a)} = -u_{p(b)} / \sqrt{3} + u_{p(c)} / \sqrt{3}$$
$$w_{q(b)} = \sqrt{3}u_{p(a)} / 2 + (u_{p(b)} - u_{p(c)}) / 2\sqrt{3} \quad (3)$$
$$w_{q(c)} = -\sqrt{3}u_{p(a)} / 2 + (u_{p(b)} - u_{p(c)}) / 2\sqrt{3}$$

B. tNTD-PLL Algorithm

tNTD-PLL shown in Fig. 2(a), adds extra delay of Ts/4 to the transformation-matrix (TM) to produce $\cos(\hat{\theta})$ from $\sin(\hat{\theta})$ the Park TM, RPT $(\hat{\theta})$ for the NTD-PLL is stated as (4).

$$R_{PT}(\hat{\theta}) = \begin{bmatrix} -\sin(\hat{\omega}(-T_s/4+t)) & \sin(\hat{\omega}) \\ -\sin(\hat{\omega}) & -\sin(\hat{\omega}(-T_s/4+t)) \end{bmatrix} = \begin{bmatrix} -\cos(-\Delta\hat{\omega}(T_s/4+\hat{\theta}) & \sin(\hat{\omega}) \\ -\sin(\hat{\omega}) & -\cos(-\Delta\hat{\omega}(T_s/4)+\hat{\theta}) \end{bmatrix} \quad (4)$$

Where in $\hat{\theta} = \int \hat{\omega} * dt = \int (\omega_n + \Delta\hat{\omega})dt = \omega_n t + \int \Delta\hat{\omega}\, dt$ (5)

where $\omega_n = 2\pi / T_s$, The TM-R_{mPT} $(\hat{\theta})$ for the PLL on mNTD- is stated as

$$R_{mPT}(\hat{\theta}) = \begin{bmatrix} \cos(\hat{\theta}) & \sin\left(-\Delta\hat{\omega}(T_s/4)+\hat{\theta}-\hat{\theta}\right) \\ -\sin\left(-\Delta\hat{\omega}(T_s/4)+\hat{\theta}-\hat{\theta}\right) & \cos(\hat{\theta}) \end{bmatrix} \quad (6)$$

To eliminate the DFOE term in both loops, use υ_d and υ_q from mNTD-PLL and NTD-PLL respectively. To realize the TM, use the first and second rows of (11) and (13), respectively.

$$R_{dPT}(\hat{\theta}) = \begin{bmatrix} \cos\left(\hat{\theta}-\Delta\hat{\omega}(T_s/4)\right) & \sin\left(\hat{\theta}\right) \\ -\sin\left(\hat{\theta}-\Delta\hat{\omega}(T_s/4)\right) & \cos\left(\hat{\theta}\right) \end{bmatrix} \quad (7)$$

To express the in-phase signal υ_α, use the equation

Let the in-phase signal, V_α be expressed as

$$v_\alpha(t) = V_m \cos(\omega_g t) = (V_n + \Delta V_m)\cos(\theta_g) = v_g(t) \quad (8)$$

where grid voltage=υ_g, V_m=amplitude and phase angle=θ_g. The term θ_g is defined as

$$\theta_g = \int \omega_g dt = \int (\omega_n + \Delta\omega i)dt = \theta_n + \Delta\theta_g \quad (9)$$

Supply frequency $(\omega_g)=\omega_n+\Delta\omega_i$, where $\Delta\omega_i$ is the frequency variation from the rated (in rad/s). The frequency, amplitude of nominal voltage, and phase are represented by ω_n, V_n, and θ_n, respectively. ΔV_m and $\Delta\theta_g$ show the phase disruption and

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magnitude of the supply voltage waveform respectively. The delay block output waveform(υ_β) with frequency drift equals

$$V_\beta(t) = \cos(\omega_g(t - T_s/4)\left(V_m(-T_s/4 + t)\right)$$
$$= \cos\left(\theta_n - \frac{\pi}{2} + \Delta\omega i(-T_s/4 + t)\right)\left(V_n + \Delta V_m(-T_s/4 + t)\right) \quad (10)$$
$$= (V_n + \Delta V_m^d)\sin(\theta_n + \Delta\theta_g^d)$$

Where $\Delta V_m^d = \Delta V_m(\Phi) \; and \; \Delta\theta_g^d = \Delta\theta_g(\Phi)$, Using $\hat{\theta} = \theta_n + \Delta\hat{\theta}$ and $\Delta\hat{\theta}^d = \Delta\hat{\theta}(\Phi)$, where $t - T_s/4 = \Phi$ The DFI-TD-based PT of NTD-PLL in (11) can be stated as

$$\begin{bmatrix} V_d(t) \\ V_q(t) \end{bmatrix} = \begin{bmatrix} \cos(\Upsilon) & \sin(\Upsilon) \\ -\sin(\Upsilon) & \cos(\Upsilon) \end{bmatrix}\begin{bmatrix} V_\alpha(t) \\ V_\beta(t) \end{bmatrix} \quad (11)$$

Where $\Upsilon = \theta_n + \Delta\hat{\theta}^d$, Under the quasi-locked state, presumptuous $\Delta\hat{\theta} \approx \Delta\theta_g, \Delta\theta_g^d \approx \Delta\hat{\theta}^d \; and \; \Delta V_m \approx \Delta\hat{V}_m$ and using equations (12) and (13), respectively. [Ref.16]

$$V_d(t) = \left(V_n + \Delta V_m^d\right)\sin(\theta_n + \Delta\theta_g^d)\sin(\theta_n + \Delta\hat{\theta}) +$$
$$= \left(V_n + \Delta V_m\right)/2\left[\cos(-\Delta\hat{\theta}^d + \Delta\theta_g) + \cos(\Delta\hat{\theta}^d + 2\theta_n + \Delta\theta_g)\right] \quad (12)$$
$$+\left(V_n + \Delta V_m^d\right)/2\times\left[-\cos(2\theta_n + \Delta\theta^d{}_g + \Delta\hat{\theta}) + \cos(\Delta\theta_g^d - \Delta\hat{\theta})\right]$$

$$V_q(t) = -(V_n + \Delta V_m)\cos(\theta_n + \Delta\theta_g)\sin(\theta_n + \Delta\hat{\theta}_g^d) +$$
$$\left(V_n + \Delta V_m^d\right)\sin(\theta_n + \Delta\theta_g^d)\cos(\theta_n + \Delta\hat{\theta}) \quad (13)$$
$$= \left(V_n + \Delta V_m\right)/2\left[-\sin(2\theta_n + \Delta\theta_g + \Delta\hat{\theta}^d) + \sin(\Delta\theta_g - \Delta\hat{\theta}^d)\right]$$
$$+\left(V_n + \Delta V_m^d\right)/2\times\left[-\sin(2\theta_n + \Delta\theta^d{}_g + \Delta\hat{\theta}) + \sin(\Delta\theta_g^d - \Delta\hat{\theta})\right]$$

C. Reference Load Voltages

The average active ($v_{sp(a)}, v_{sp(b)} \& v_{sp(c)}$) and reactive ($v_{sq(a)}, v_{sq(b)} \& v_{sq(c)}$) components are calculated using of fundamental three-phase source voltages ($v_{s(abc)}$), quadrature-phase unit templates ($w_{q(abc)}$) and in-phase unit templates ($u_{p(abc)}$) are calculated using tNTD-PLL equations (12) and (13)

$$v_{sp(avg)} = \frac{v_{sp(a)} + v_{sp(b)} + v_{sp(c)}}{3} \quad (14)$$

$$v_{sq(avg)} = \frac{v_{sq(a)} + v_{sq(b)} + v_{sq(c)}}{3} \quad (15)$$

The dc-bus voltage (sensed) is subtracted from voltage of dc-bus (reference) and is calculated as,

$$v_{dc(err)} = v_{dc(ref)} - v_{dc} \quad (16)$$

The output equation for PI controller (dc) is given as,

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$$v_{L(p)(n)} = (-v_{dc(err)(n-1)} + v_{dc(t)(err)(n)})k_{p(1)} + v_{dc(err)(n)}\, k_{i(1)} + v_{L(p)(n-1)} \quad (17)$$

The magnitude of terminal voltage is calculated as

$$v_{s(t)} = \sqrt{2(v_{s(c)}^2 + v_{s(b)}^2 + v_{s(a)}^2)/3} \quad (18)$$

The error value obtained by subtracting eqn (18) from terminal voltage (reference) and calculated as

$$v_{s(t)(err)} = v_{s(t)(ref)} - v_{s(t)} \quad (19)$$

The equation of output for ac PI controller is given as

$$v_{L(q)(n)} = (-v_{s(t)(err)(n-1)} + v_{s(t)(err)(n)})k_{p(2)} + v_{s(t)(err)(n)}\, k_{i(2)} + v_{L(q)(n-1)} \quad (20)$$

The active component (ref) of load voltage is given from eqn (14) and eqn (17)

$$v_{Lp}^{*} = v_{sp(avg)} + v_{L(p)} \quad (21)$$

The reactive component (ref) of load voltage is given from eqn (15) & eqn (19)

$$v_{Lq}^{*} = v_{sq(avg)} + v_{L(q)} \quad (22)$$

The active reference load voltages can be acquired by

$$\begin{aligned} v_{Lp(a)}^{*} &= u_{p(a)} \times v_{L(p)}^{*} \\ v_{Lp(b)}^{*} &= u_{p(b)} \times v_{L(p)}^{*} \\ v_{Lp(c)}^{*} &= u_{p(c)} \times v_{L(p)}^{*} \end{aligned} \quad (23)$$

The reference quadrature load voltages can be acquired by

$$\begin{aligned} v_{Lq(a)}^{*} &= w_{q(a)} \times v_{L(q)}^{*} \\ v_{Lq(b)}^{*} &= w_{q(b)} \times v_{L(q)}^{*} \\ v_{Lq(c)}^{*} &= w_{q(c)} \times v_{L(q)}^{*} \end{aligned} \quad (24)$$

The load voltages (reference) can be estimated as

$$\begin{aligned} v_{L(a)}^{*} &= v_{Lq(a)}^{*} + v_{Lp(a)}^{*} \\ v_{L(b)}^{*} &= v_{Lq(b)}^{*} + v_{Lp(b)}^{*} \\ v_{L(c)}^{*} &= v_{Lq(c)}^{*} + v_{Lp(c)}^{*} \end{aligned} \quad (25)$$

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The error voltages are difference of load voltages (sensed) and load voltages(reference), which are compared 10 kHz frequency PWM to generate switching pulses to DVR.

IV. ANT LOIN OPTIMIZATION

The optimization technique is used to acquire the accurate PI gains to extract the fundamental load voltages. The proper extraction depends on tNTD-PLL and gains acquired from optimization technique.

The optimization technique is required to run before the actual DVR system runs,

Cost function = integral (e^2t.dt) (23)

Where 'e' is the error input of AC PI and AC PI controllers

The gains obtained from optimization technique is shown in Fig. 4(a), 4(b) and 4(c) and given as K_{i1}=4.53, K_{i2}=3.61, K_{p1}=3.50 and K_{p2}=3.41 and cost function convergence value = 241.

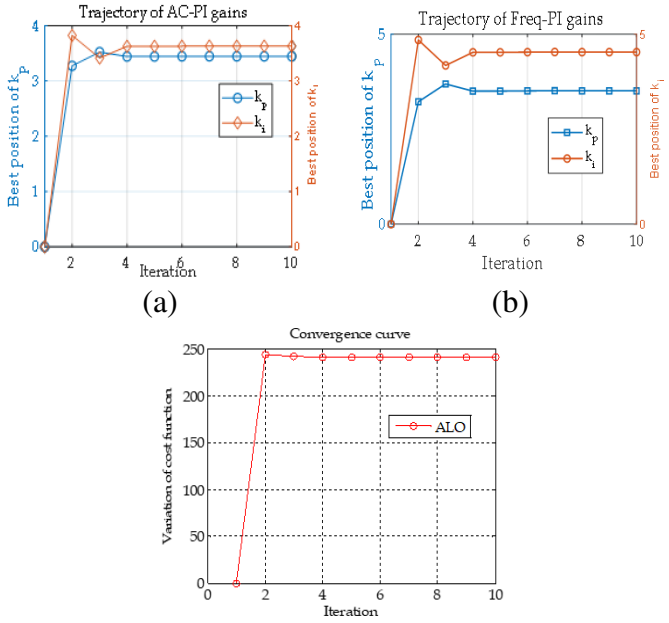

Fig. 4 (a) AC PI gains (b) DC PI gains (c) Cost Function

V. DISCUSSION OF SIMULATION RESULTS

Figs. 5-8 shows the load voltages, source voltages, injected DVR voltages, reference with sensed terminal voltage, dc bus voltage (sensed) with reference, and source currents with swell, sag, unbalance and harmonics occurrence.

Fig 5 illustrates the performance waveforms of DVR under swell event with tNTD algorithm, the swell of 10% of 415V (rms) = 41.5V (rms) is created in source voltage from 3.4 sec to 3.6 sec.

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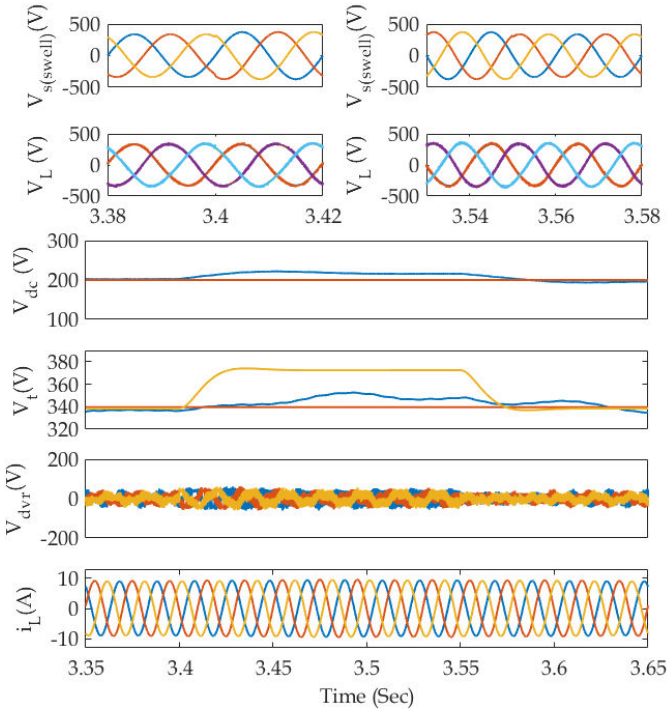

Fig. 5 Performance waveforms with swell

It can be observed in Figs 5(a) & 5(c) from 3.38sec to 3.42sec and in Figs 5(b) & 5(d) from 3.43sec to 3.58sec the enlarged windows of supply voltage and load voltage superimposed on reference load voltages. Fig. 5(e) depicts the reference and sensed dc bus voltage of dc bus; Fig. 5(f) shows the terminal voltage and reference terminal voltage and Fig. 5(g) shows the currents in distribution system.

During of sag operation, even when the source voltage is excess of 41.5V, but the voltage of load is constant at rated voltage and exactly following the reference load voltage. The DVR is injects anti-phase voltage with source, all over this process, the dc-link voltage is modulated to value of 200V, and the terminal voltage is adjusted to 339.6.

current.

Fig. 6 depicts the performance waveforms of a DVR during a swell event using a tNTD algorithm; a sag of 10% of 415V (rms) = 41.5V (rms) is formed in the source voltage from 3.4 to 3.6 seconds.

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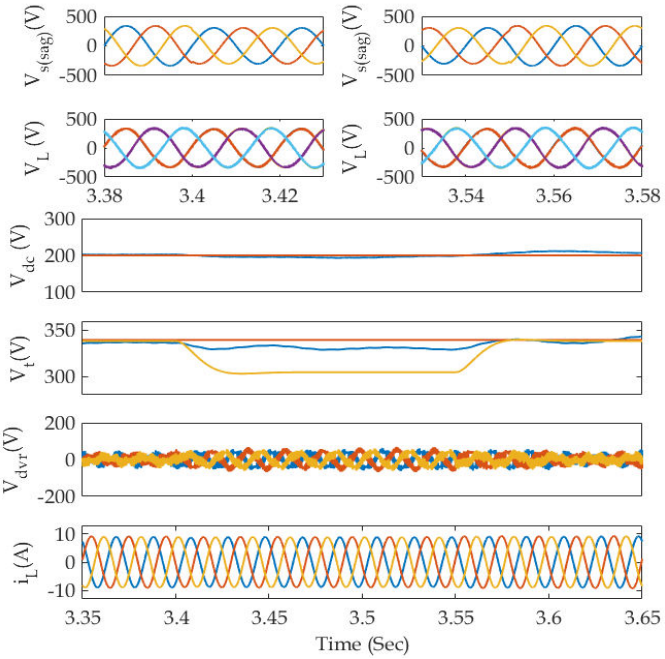

Fig. 6 Performance waveforms with sag

The larger windows of supply voltage and load voltage superimposed on reference load voltages may be seen in Figs 6(a) & 6(c) from 3.38 sec to 3.42 sec, as well as in Figs 6(b) & 6(d) from 3.43sec to 3.58sec. Fig. 6(e) displays the sensed and reference dc-bus voltage; Figure 6(f) displays the terminal voltage and terminal voltage (reference); and Figure 6(g) displays the distribution system currents.

During sag operation, even when the source voltage is less than 41.5V, the load voltage remains constant at the rated voltage and precisely matches the reference load voltage. The VSC (DVR) injects in-phase voltage to source throughout the operation, modulating the voltage of dc-link to a steady 200V and adjusting the terminal voltage of load to a regulated 339.6 V (peak of phase voltage).

Fig. 7 shows the DVR performance waveforms of unbalance event utilizing a tNTD control algorithm, an unbalance of 89.6V in phase 'C' is introduced into the source voltage from 3.4 to 3.6 seconds. Figs. 7(a) & 7(c) show selective windows of supply voltage and load voltage superimposed on reference load voltages from 3.38 sec to 3.43 sec, as do Figs. 7(b) & 7(d) from 3.43sec to 3.58sec. Fig. 7(e) shows sensed dc-bus and reference voltage of dc-bus, Fig. 7(f) shows the sensed & reference terminal voltage and Fig. 7(g) shows the distribution system currents. During unbalance event, even when the unbalance of 89.6V in phase 'C', the load voltage remains constant at the rated voltage and precisely matches the reference load voltage. The phase 'C' of DVR injects deficient voltage into the source throughout the operation to regulate the load voltage, modulating the dc-link voltage to controlled 200V and adjusting the load voltage (terminal) to a steady 339.6 V.

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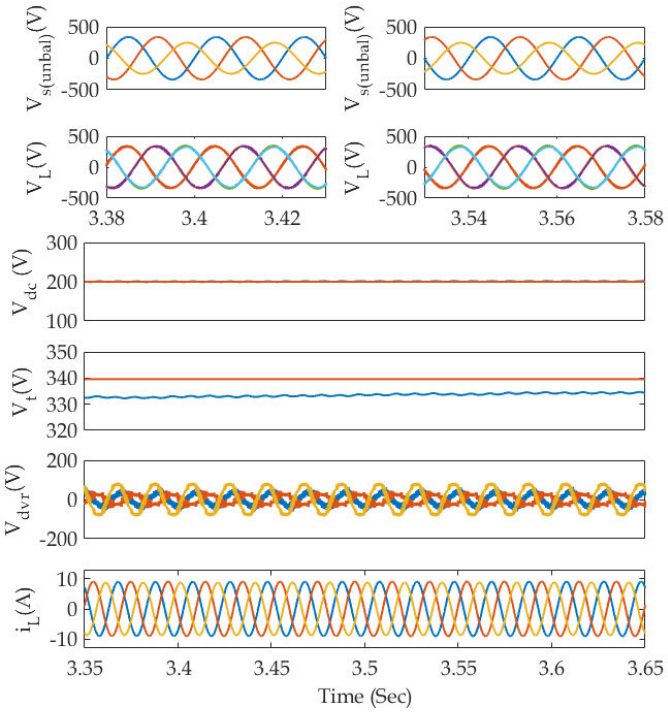

Fig. 7 Performance waveforms with unbalance

Fig. 8 shows the DVR performance waveforms with harmonic event utilizing a tNTD control algorithm, a distortion of 9.68% THD is introduced into the source voltage from 3.4 to 3.6 seconds. Figs. 8(a) and 8(c) display selective windows of supply voltage and load voltage superimposed on reference load voltages from 3.38 sec to 3.43 sec, as do Figs. 8(b) & 8(d) from 3.43sec to 3.58sec. Fig. 8(e) shows the sensed and reference voltage of dc bus, Fig. 8(f) displays the sensed and reference terminal voltage and Fig. 8(g) shows the distribution system currents.

During harmonic event, even when the voltage of source is distorted, the voltage of load remains constant and undistorted and follows the reference load voltage. The DVR injects anti harmonic voltages into the source throughout the operation to regulate the load voltage, modulating the voltage of dc-link to a regulated 200V and adjusting the load voltage (terminal) to a controlled 339.6 V.

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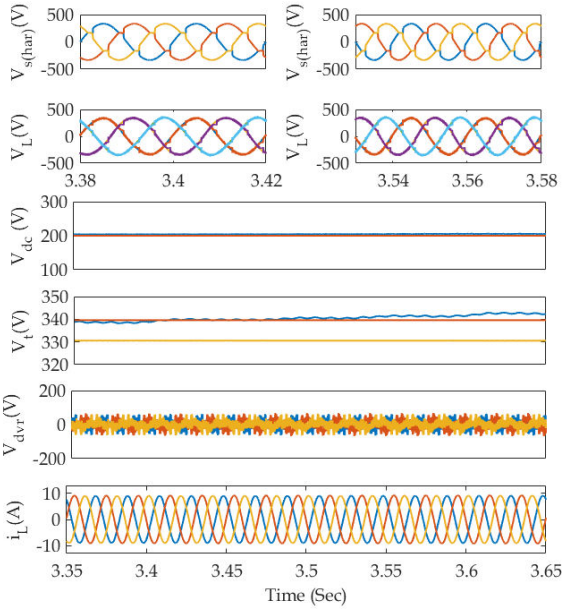
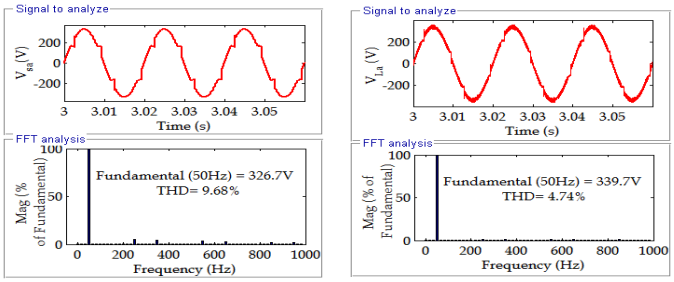


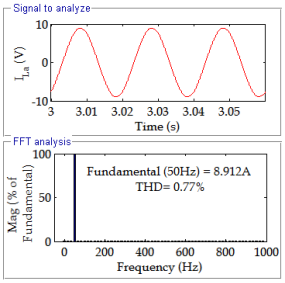
Fig. 8 Performance Waveforms with harmonics

The tNTD-PLL is highly effective in decreasing offset and double-frequency oscillatory errors, as well as noise, phase jitter, and frequency drift. The control algorithm was effective in achieving the intended results.

Fig. 9 (a) and (b) illustrate the harmonics in the source and load voltages. The voltage of grid possesses distortions with a THD of 9. 68 % while the load voltage and load current bears harmonics with a THDs of 4.74 % and 0.77% respectively, which are well within the limits of IEEE standards.



(a) (b)



(c)

Fig. 11 Harmonic Spectra (a) Source voltage (b) load voltage (c) load current

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VI. Discussion of Hardware Results

A. Performance of DVR with Hardware

Fig. 12 demonstrates the prototype of DVR is designed and developed on d-SPACE MicroLab box in laboratory and the experimental results are presented. Fig. 12 (a-f) displays the supply voltage, load voltage, DVR voltage, power of the load, THD of load voltage and current.

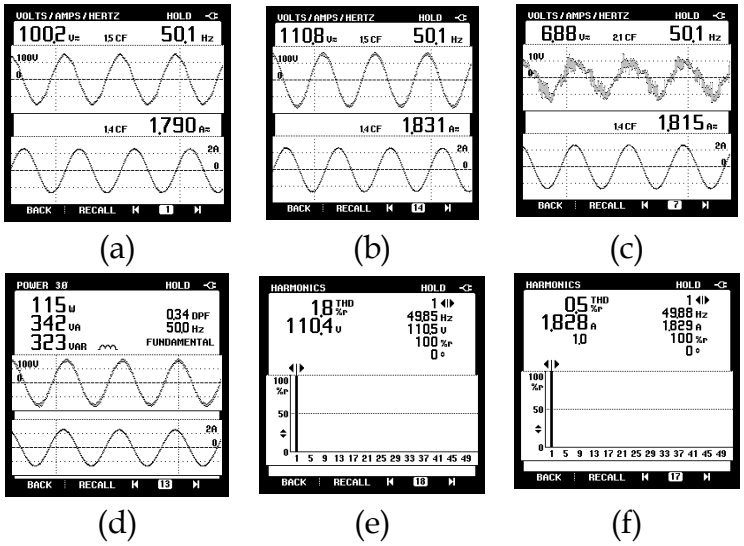

Fig. 12 Hardware results of sag (a) source voltage (b) load voltage (c) DVR voltage (d) Power (e) Harmonic spectra of load voltage (f) Harmonic spectra of current

Throughout dip in supply the VSC drives an voltage in-phase to the supply voltage so as to regulate the load voltage is regulated at 110V (rated value). The load voltage with a THD of 1.8% and source current with a THD of 0.5 % which are well within IEEE standards.

B. Dynamic Performance with Hardware

Fig. 13 (a)-(c) displays the dynamic performance of DVR with tNTD-PLL algorithm. As the supply voltage dips by 11V, the DVR intervenes by precisely injects the nuanced voltage component that aligns nicely with the supply voltage direction. This in-depth composition promises that the load voltage is consistently controlled at 110V, as specified by its rated value. Despite the transient nature of supply voltage disturbances, the load enjoys a stable situation, with a small harmonic distortion of 1.8% on the voltage and a moderate 0.5% harmonic distortion on the current. The tNTD-PLL introduces a delay element into the PLL's feedback loop, increasing transfer latency but reducing double frequency oscillatory and offset faults. er than the target frequency. Such operation not only demonstrates the DVR's effective operation of tNTD-PLL algorithm and the PI control gains are optimized by ALO technique, but also emphasizes its adherence to established by the IEEE-519 standards.

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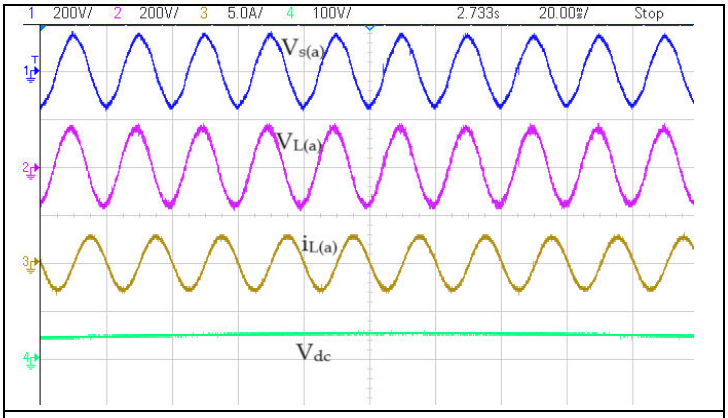
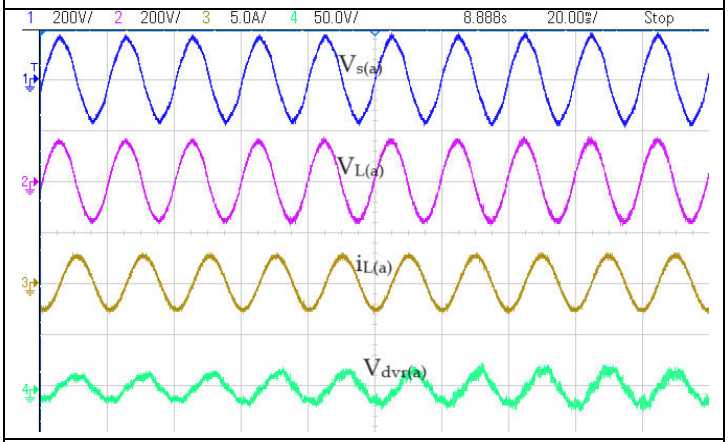


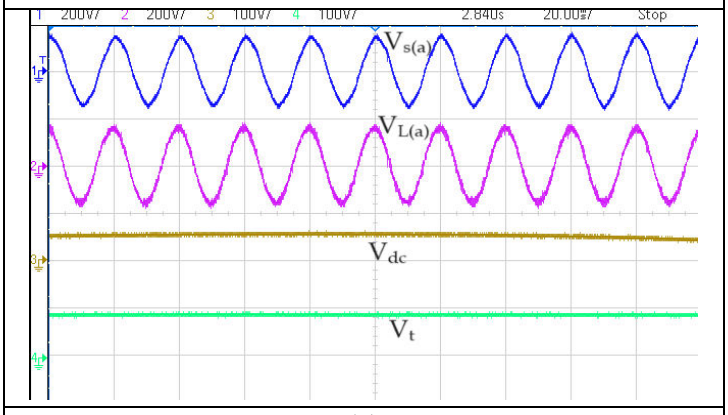
(a)

Axis-X- 20ms/div, Axis-Y-Ch-1&2: 200V/div, Ch-3&4: 5 A/div & 100V/div



(b)

Axis-X- 20ms/div, Axis-Y-Ch-1&2: 200V/div, Ch-3&4: 5 A/div & 50V/div



(c)

Axis-X- 20ms/div, Axis-Y-Ch-1&2: 200V/div Ch-3&4: 5 100V/div

Fig. 13 Dynamic performance of DVR

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VII. CONCLUSIONS

The study addresses voltage-based power quality issues at the load end in case of swell, distortion, sag, and supply voltage unbalance. The efficacy of the proposed tNTD-PLL control strategy is carried out with MATLAB simulations, study done for such as swell, sag, supply voltage unbalance and distortion. The proposed strategy is quicky responds to all the PQ issues mentioned above and it is efficiently extracts the fundamental from the distorted waveforms. The tNTD-PLL is extremely effective at reducing offset and double-frequency oscillatory errors, as well as noise, phase jitter, and frequency drift. The control strategy is working well and giving the expected results. The PI tuning is done by using ALO, it can be detected that speed of tuning of PI-controller gains is improved compared the conventional tuning. The optimized gains obtained from ALO technique is applied to PI controller regulate voltage of dc-bus at a steady 200V and voltage of terminal is maintained at controlled value of 339.6V (rms) rated value. The tNTD-PLL strategy-based for DVR during compensation of distortions, source voltage is having a distortion of 9.68% whereas load voltage is having a distortion of 4.74% in simulation, which are well within standards of IEEE-519. The simulation results are validated using developed prototype using d-SPACE MicroLab Box. The hardware results of DVR with sag are studied and performance is quite satisfactory using tNTD-PLL control algorithm.

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