International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

A MODIFIED THREE-STAGE COMPARATOR WITH QUICK SPEED AND MINIMAL KICKBACK

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Abstract: This short introduces a three-stage comparator along with a modified version that reduces kickback noise and increases speed. The three-stage comparator used in this study contains an additional amplification step, which boosts speed and voltage gain when compared to conventional two-stage comparators. The three-stage comparator allows for the use of nMOS input pairs in both the regeneration stage and the amplification stage, further boosting speed, in contrast to the conventional two-stage construction that employs pMOS input pair in the regeneration stage. Furthermore, a CMOS input pair is used at the amplification step in the suggested modified version of the three-stage comparator. By cancelling out the nMOS kickback via the pMOS kickback, this significantly lowers the kickback noise. In the regeneration stage, it also provides an additional signal line, which aids in accelerating the pace even further. The suggested three-stage comparator and the traditional two-stage comparator are both built in the same 130-nm CMOS technology for ease of comparison. According to measured data, the redesigned three-stage comparator increases speed by 32% and reduces kickback noise by a factor of 10. Noise or input referred offset are not sacrificed in order to achieve this improvement.

Index Terms: low kickback, fast speed, comparator.

1. INTRODUCTION

A fundamental component of many kinds of analog -to-digital converters (ADCs), the comparator is crucial [1], [2]. Specifically, with high-speed, high-resolution SAR ADCs, the comparator speed, offset, kickback noise, and input referred noise all restrict the ADC sampling rate and accuracy. It is crucial to create a high-performance comparator under these conditions. In recent years, a large number of comparator structures have been reported. The classic construction seen in [3] and [3] is the Strong ARM latch. It offers a number of benefits, including rail-

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to-rail outputs, no static power, and quick comparison because of the positive feedback [3]. However, it also has a number of drawbacks. First, the tiny current source underneath the latch restricts the pace of its regeneration. In this case, the input pair of transistors is the current source. The current in the current source is restricted as a result of the input pair's common-mode input of VDD/2, which also restricts the regeneration speed. Second, a high-power supply voltage is required since there are several stacked transistors. These problems do not affect two-stage comparators. [11]–[5]. Consider the two-stage comparator constructed by Miyahara in [9] (see Fig. 1). The little current source no longer restricts the rate of regeneration. This is due to the fact that the gate-source voltage of its latch input pair, M6–M7, is two times greater than the VDD/2 of the StrongARM latch. Reducing the quantity of stacked transistors is an additional benefit. As a result, the power supply voltage need is loosened.

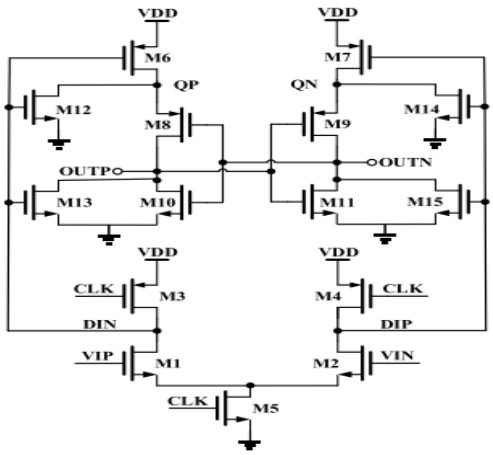

Fig. 1. Miyahara's two-stage comparator.

Even while the Miyahara's two-stage comparator quickens things, there are still ways to make it faster. Its latch input pair M6-7, which are pMOS transistors, are shown in Fig. 1. The regeneration speed is limited by the tiny (2–3 times lower) pMOS hole mobility compared to the nMOS electron mobility. Our objective is to significantly increase the regeneration speed by switching to nMOS transistors for the latch input pair. For the preamplifier input pair, we must preserve the nMOS transistors in the interim.

This brief provides a three-stage comparison in order to do this. The nMOS input pairs may be used for the latch-stage and the first-stage preamplifier by adding an additional preamplifier stage, which increases the regeneration speed. Additionally, these input pairs ensure a low input referred noise by operating in the saturation area at the start of the comparison. Voltage gain, which is another function of the additional preamplifier stage, aids in accelerating regeneration and reducing noise and input referred offset. The three-stage comparator used in this study is quicker and has less input referred noise than the previous three-stage comparator from [12].

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ISSN: 2457-0362

A three-stage comparator that has been adjusted is also suggested in this brief. At the first-stage preamplifier, kickback noise is significantly decreased by employing a CMOS input pair. In the latch stage, an additional route is additionally introduced in order to minimise the noise and input referred offset while also accelerating regeneration. When compared to the traditional two-stage comparators, the three-stage comparator used in this study enhances speed by 25% when implemented in the same 130 nm process. However, the updated version that is suggested boosts speed by 32% and reduces kickback noise by 10 times.

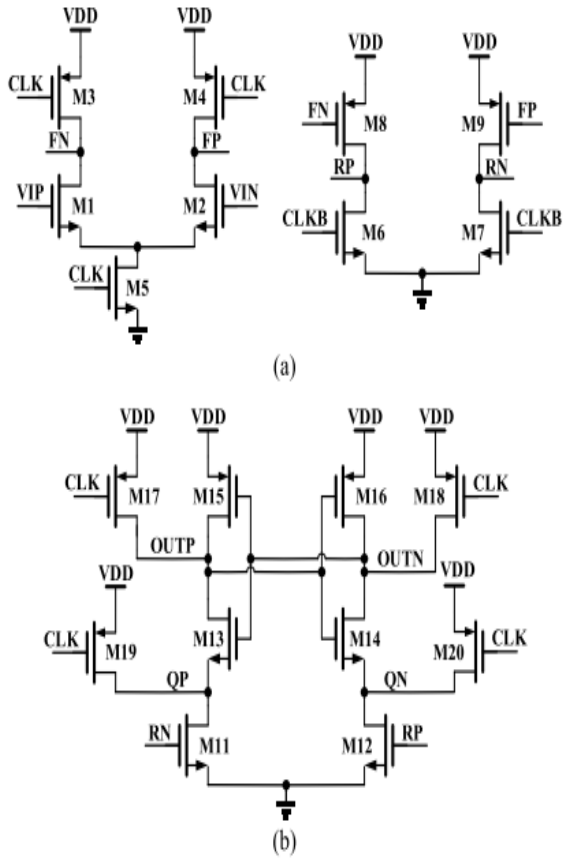

Fig. 2. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

2. THREE-STAGE ANALYZER

A. Two-Stage Comparator Review

The Miyahara two-stage comparator is seen in Fig. 1. The operating system consists of three distinct phases: reset, amplification, and regeneration. When CLK = 0, the comparator is reset during the reset phase. The input signal VIP–VIN is amplified and delivered to the latch stage during the amplification phase (CLK = 1).

OUTP and OUTN regenerate to VDD or GND during the regeneration phase. As previously shown, a structure of this kind is limited to pMOS input pairs at the latch stage.

A. Three-Step Equivalency

In this study, a three-stage comparator is shown in Fig. 2. The three phases are interconnected in that order. The primary difference with Miyahara's counterpart is the addition of a second stage, or an additional preamplifier. By acting as an inverter, this additional preamplifier allows the latch stage to utilise the nMOS input pair M11–12 rather than the pMOS input pair, increasing speed.

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Additionally, the additional preamplifier offers voltage gain, which increases regeneration speed and reduces noise and input referred offset.

Although the additional preamplifier helps in speeding up the process, the additional stage itself adds to the delay as the amplified signal must pass through two stages as opposed to one before reaching the latch stage. Therefore, it is important to deliberate on whether the benefits of this additional delay outweigh the costs. Its outputs FP and FN fall to GND after the first-stage amplification, as shown in Fig. 2. Consequently, the massive gate-source of the second-stage input pair M8–9 is created.

Table 3. Temporal simulated waveforms of the three-stage comparator and the comparator made by Miyahara.

voltage that matches VDD. Because of this, M8–9 has a current that is strong enough to rapidly draw up RP and RN. This indicates that in comparison to the latch stage's significant delay (about 200 ps in post-layout simulation), the additional delay caused by the second stage is little (around 20 ps). This makes sense since the second stage is essentially a low-delay dynamic inverter. Furthermore, the first-stage output load in the three-stage comparator is only M8–9 in Fig. 2, as opposed to the first-stage output load in the Miyahara comparator (M6-7 and M12–15 in Fig. 1). The amplification speed is increased by many times when the output load is lowered.

3. SUGGESTIVE EDITION OF THE THREE-STAGE COMPARATOR

A: Circuit Architecture

Figure 3 illustrates the updated three-stage comparator that this brief suggests be used to further increase speed and decrease kickback noise. The improved version contains additional routes M29–32 in the latch stage of Fig. 3(c) and the extra first two stages of Fig. 3(b) compared to the original version in the preceding section. The additional pair of stages uses pMOS input.

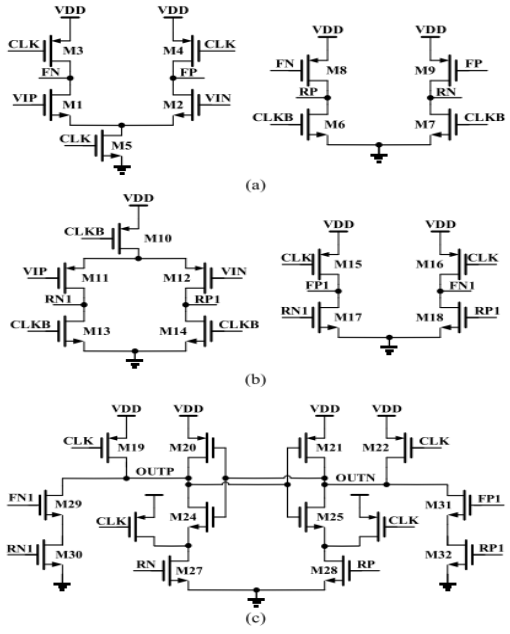

Fig. 3. Proposed modified version of three-stage comparator. (a) Original first two

stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to eliminate the kickback noise of the nMOS input pair M1-2.

Additionally, the additional routes M29–32 provide an additional signal to the latching nodes OUTP and OUTN, which increases regeneration speed and significantly suppresses noise and input referred offset.

These additional circuits function as follows. After the reset, CLK is equal to 0 and CLKB to 1. In Fig. 3(b), FP1 and FN1 are reset to VDD, while RP1 and RN1 are reset to GND. In Fig. 3(c), this disables M30 and M32, guaranteeing that the additional route M29–32 is free of static current.

CLK increases to 1 and CLKB decreases to 0 during the amplification phase. In Fig. 3(b), RP1 and RN1 increase to VDD (where R denotes rise).

Next, FP1 and FN1 fall to GND, where F denotes fall. The additional routes in Fig. 3(c) are switched on for a brief period of time, drawing a differential current from the latching nodes OUTP and OUTN, since the rising of RP1 and RN1 happens before the falling of FP1 and FN1.

As a result, there is a differential voltage at OUTP and OUTN, which suppresses noise and the comparator input referred offset and speeds up the regeneration phase thereafter. To stop the static current, the additional pathways in Fig. 3(c) are shut off once again once FP1 and FN1 fall to GND.

tt corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	219.93 ps	215.61 ps	170.98 ps	151.85 ps
1 mV	266.37 ps	277.25 ps	213.97 ps	189.52 ps
ff corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	166.36 ps	168.14 ps	137.21 ps	116.18 ps
1 mV	207.10 ps	226.06 ps	180.47 ps	153.46 ps
ss corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	306.60 ps	306.18 ps	229.85 ps	193.80 ps
1 mV	373.41 ps	383.27 ps	264.51 ps	225.31 ps

Table I Comparator Delay Versus Input Voltage Under Different Corners (Vcm = 600 Mv).

4. SIMULATED AND MEASURED RESULTS

A. Post-Layout Simulated Results

This section compares the three-stage comparators of this work with the two-stage comparators of Miyahara's comparator [9] (Fig. 1) and Elzakker's comparator [11]. For fair comparison, all comparators are post-layout simulated under the same 130-

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nm process. All comparators are also designed with the same input referred noise of 440 μV, so that other specifications can be compared. Table I shows the delay at 90% settling. The common-mode input Vcm is set to 0.6 V. As can be seen, the delay of three-stage comparators is smaller than the two-stage comparators by 15%–25% under all conditions. Meanwhile, the delay of modified version is smaller than the original version by 10%–18%.

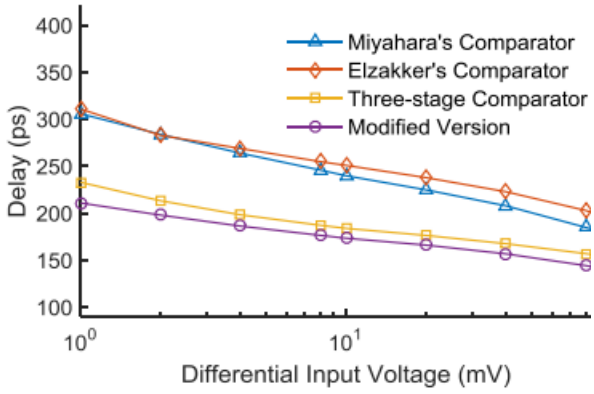

Fig. 4. Measured delay versus differential input voltage.

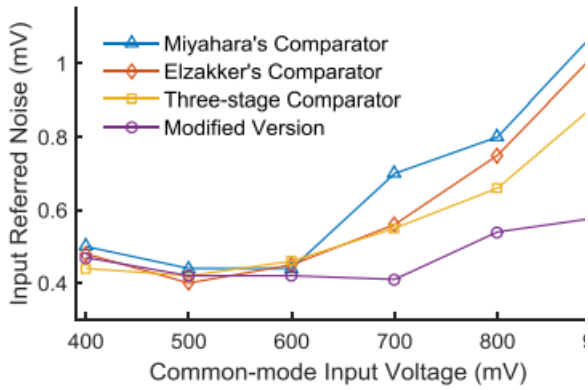

Fig. 5. Measured input referred noise versus common-mode input voltage

5. CONCLUSION & FUTURE WORK

The benefits of a three-stage comparator—which comes with a modified version—include minimal kickback noise, rapid speed, and low input referred offset and noise. These comparators work well with high-resolution, high-speed SAR ADCs. Ultimately, quantifiable outcomes confirm how useful these comparators are.

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