International Journal For Advanced Research In Science & Technology
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DESIGN AND IMPLEMENTATION OF NOVEL SRAM MEMORY ARRAY WITH HIGH SECURITY

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ABSTRACT: There is an ever increasing need for running various multimedia and computer based applications on a variety of popular digital systems. SRAM cell acts as a memory to store the data. In this project design and implementation of novel SRAM memory array with high security is implemented. The main intent of this project is to reduce the delay and improve the performance of system. Initially PRPG (Pseudo Random Pattern Generator) will generate the test patterns. If there are any errors in obtained data cyclic redundancy check (CRC) will detect and correct it and gives the accurate data. Address control unit decodes address of data in two ways they are row decoder and column decoder. Row decoder decodes the data in row format and column decoder will decodes the data in column format. At last the row and column data will be saved in SRAM array memory. From this data will perform read and write operations. This is simulated using Xilinx technology. From simulation results it can observe that effective output is obtained in terms of delay and area.

KEYWORDS: SRAM memory array, multimedia, CRC, PRPG, delay and area.

I. INTRODUCTION

In designing a system, area and power consumption are very important in VLSI. Memory is a crucial part of the whole device and draws a lot of energy from the supply in order to perform and store data. Thus, there is a need to reduce the energy consumption in digital circuits and since memory cells draws a lot of supply in order to process and store data, applying various techniques to improve their efficiency in energy consumption is desired [1]. Also the time of execution is low because SRAM and ROM are to be connected through external device.

Due to this area will be increased which leads to increase in power and cost. In this memory chip instead of RAM we are using SRAM where it automatically refresh it data for the particular time period.

The ever increasing need for high performance VLSI chips demands higher on-die SRAM requirements. As a consequence, efficient SRAM scaling assumes importance in today's VLSI design applications. Scaling the supply voltage further affects the SRAM cell stability [2]. To reduce the gate tunneling leakage current in digital circuits, several techniques were tried in the past. Some techniques involve application of lower than normal gate voltage to reduce the gate leakage and changing the ground voltage during the period of inactivity so as to reduce the sub threshold leakage.

SRAM-based FPGA stores rationale cells setup information in the static memory sorted out as a variety of hooks. FPGA is utilized for structuring complex advanced circuits [3]. Power utilization is likewise decreased by utilizing SRAM. The SRAM shifts power utilization depend upon how every now and again it is gotten to; it very well may be as eager for power as unique RAM, at full data transmission when it is utilized at high frequencies a few ICs can devour numerous watts. At slower pace the RAM is utilized, for example, in applications with Moderately timed chip, draws next to no power and can have an about insignificant power utilization when

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

sitting inert – in the district of a couple of small scale watts [4].

A few strategies have been actualized to oversee control utilization of SRAMbased memory structures. FPGA gadget adaptable by SRAM comprises of a variety of programmable rationale squares interconnected by a programmable directing system and I/O squares. SRAM-based FPGA gadgets are getting to be mainstream due to their elite, decreased improvement cost and reprogram ability. FPGA's dependent on a nanometer innovation with denser joining plans. Recollections are a standout amongst the most generally utilized components in electronic frameworks. Radiation in the earth genuinely influences the usefulness of a circuit. A soft error upset (SEU) happens when a charged molecule, present in nature, hits the silicon of a circuit presenting a blunder in the framework. Such mistakes in FPGA gadget influences the usefulness of the mapped structure additionally called as Soft blunders [5].

The rationale blend and circuit configuration results in the circuit parts, which are separated from a physical library and changed over into rectangular shapes with fixed measurements. The planning imperatives on sign proliferation ways along nets are characterized. A total format of the circuit, where every one of the cells are situated on the chip without covering and all the interconnection ways finished, is the yield of the physical plan arrange. This format is accomplished in different stages: apportioning, floorplanning, arrangement, directing and compaction.

The impact of SRAM has grown significantly as battery-powered portable devices and low force sensor applications proliferate. The majority of SRAM plan effort has been focused on promoting voltage scaling and increasing yield. The conventionally actualized six transistor (6T) cell in SRAMs enables high thickness, bit-interleaving, and rapid differential detecting but suffers from half-select security, read-upset dependability, conflicting peruse and compose measuring, and read-upset reliability.

II. LITERATURE SURVEY

Chinmay Sharma, Varun Chhabra, Balwinder Singh, Hitesh Pahuja, et. al. [6] proposes a reversible design of 4-bit 6-T SRAM array at 180nm-1.8V CMOS technology which achieves 8% reduction in energy consumption of the circuit. The concept of reversible logic in circuit designing is garnering growing attention for low-power applications such as DNA computing, quantum computing and ultra-low power CMOS design. The designs are simulated on Cadence virtuoso 6.1.4 schematic editor. The present work also concludes with some insights on the operation of conventional SRAM 6-T cell and the feasibility of reversible logic.

M. Ramakrishnan, J. Harirajkumar, et. al. [7] presents Design of 8T ROM Embedded SRAM using Double Wordline for Low Power High Speed Application. Here 8T transmission gate based design is used to create an array 4X4 configurable random access memory and it has an extra word line to configure the certain part of RAM to ROM to act as cache memory. By using this on chip catch memory the propagation delay occurs while accessing off chip memory will be reduced, this will reduce the bottle neck to increase the speed of the processor. Due to extra word line separate address decoder logic was designed, decoder will decide which is to be consider as RAM and which is to be consider as ROM. Transmission gate

based SRAM is used to avoid the weak logic occurred while using pass transistor logic.

A. Q. Ansari and J. A. Ansari, et. al. [8] proposed a dual-Vt 7T (seven transistor) SRAM cell and compared with the standard 6T SRAM cell on the basis of read delay, write delay, leakage power consumption and Static Noise Margin (SNM) (during hold, read and write). This proposed cell uses single bitline for read and write operation. Thus it also improves the access time of the cell. The consumption of leakage power is reduced by 61.50%. Write delay is reduced by 66.67%. All the simulation work is carried out using the Eldo SPICE tool of Mentor Graphics on 65nm technology at 27°C.

K. Mehrabi, B. Ebrahimi and A. Afzali-Kusha, et. al. [9] propose a new seven transistors (7T) static random access memory (SRAM) cell that improves read stability and write ability of the conventional 6T SRAM cell. This strategy weakens the positive feedback and enhances the write ability of the cell. HSPICE Simulations in 90 nm CMOS technology show 80% and 54.9% improvement for the proposed structure with respect to the conventional 6T cell in the read stability and write ability, respectively, at the supply voltage of 500 mV. Using the virtual ground in this design causes leakage power reduction for each cell by stacking effect. The virtual ground is shared among all the cells in a row in order to lower the SRAM block power and relax the area and power overhead of extra transistor that used. The HSPICE simulation results also show 12.35% improvement in the static power at the 500 mV supply voltage.

Shashank Ranganath, Shankaranarayana Bhat M., Alden C. Fernandes et. al. [10] reports design of low leakage Static Random Access Memory (SRAM) Bit-Cell and Array. The SRAM cell and array were designed using 180nm technology and analyzed at 25°C with VDD of 1.8V using Cadence tool. The proposed SRAM cell showed an improvement of around 65% in average SPD over the 6T SRAM cell during the write '1' operation and an improvement of around 66% in average SPD over the 6T SRAM cell during the write '0' operation. Write and Read access times of the proposed 1 kB SRAM Array were recorded to be 27.92% and 25% faster than the 1 kB 6T SRAM Array respectively.

III. NOVEL SRAM MEMORY ARRAY WITH HIGH SECURITY

The below Fig. 1 shows the block diagram of proposed system. Initially input is tested unit BIST and transfers the data to SRAM control circuit block. If there are any errors in obtained data CRC will detect and correct it and gives the accurate data. Address control unit decodes address of data in two ways they are row decoder and column decoder. Row decoder decodes the data in row format and column decoder will decodes the data in column format. At last the row and column data will be saved in SRAM array memory. From this data will perform read and write operations.

SRAM Memory Array:

Low repeats movement SRAMs and their reliability are the topic of the theory. Any arbitrary concerns continue to be the driving force behind the development of new cycle cell and memory peripheral models to engage satisfying yield delivery in 32nm CMOS and earlier. The level of expertise of SRAM is examined from various angles to shed light on the difficult trade-offs between the design of the piece cell, its tasks, and the additional circuits to support the tasks, the thickness, the power use, and finally the

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ISSN: 2457-0362

success to excuse the effects of irregularity. The six-semiconductor SRAM is used as a starting point for the discussion, along with approaches that are widely used to limit the impact of arbitrariness.

Unfortunately, the efficiency of the most cutting-edge techniques to manage the power use is addressed pretty distant from the topic of the SRAMs' power consumption at this time. Finally, a design termed 8T-Portless proposes the eight-semiconductor bit-cell as an alluring alternate option. Due to their first-class characteristics, static erratic access memory (SRAM) is often widely employed; a chip may include up to 70% SRAMs in semiconductor count or area. The semiconductor industry is an example of how to strive for smaller chips and more fuse since it is more difficult and expensive to build new creative centers.

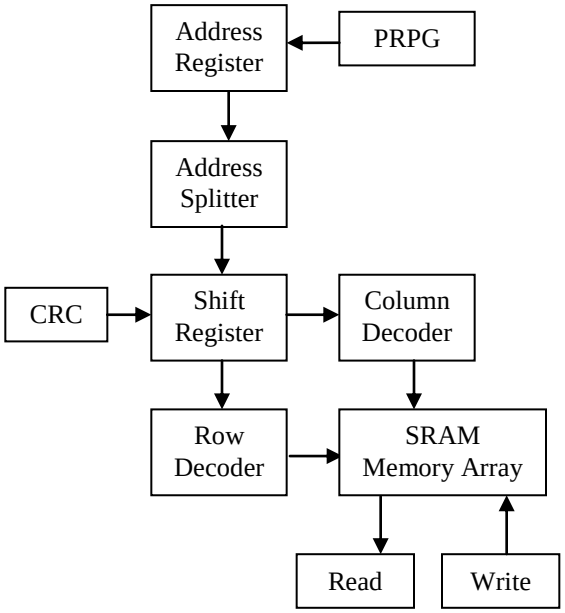

Fig. 1: BLOCK DIAGRAM OF PROPOSED SYSTEM

CRC:

An error-detection algorithm called a cyclic overt repetitiveness check is frequently used in computerized organizations and capacity devices to identify unintended modifications to raw data. Information entry blocks are given a brief tick worth in these frameworks based on the remainder of a polynomial division of their components. After recovery, the estimation is redone, and if the cheque values don't match, remedial action can be taken to prevent information tampering. For error correction, use CRCs (see bitfilters).

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Row and Column Address Decoder:

Based on the binary row and column addresses, the row and column decoders choose a particular memory position in the array. By definition, a row decoder made to operate a NOR ROM array must choose one of the 2N word lines by increasing its voltage to VOH.

IV. RESULTS

Designed SRAM memory array is simulated using Xilinx technology. The below Fig. 2 shows the RTL schematic of proposed system. A synchronous digital circuit's data movement between hardware registers and the logical operations carried out on those signals are modeled by the register-transfer level (RTL), a design abstraction. The Fig. 3 shows the technology schematic of proposed

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ISSN: 2457-0362

system. This diagram was developed following improvements and innovations with a focus on the time of union engagement. The plan is depicted in terms of the rationale components that have been added to the intended Xilinx device or "innovation"; for example, in terms of LUTs, communicate reasoning, I/O cushions, and other innovation-specific components. This schematic gives you access to a high-level representation of your HDL advanced for a certain Xilinx engineering, which may help you identify configuration concerns early on in the design interaction.

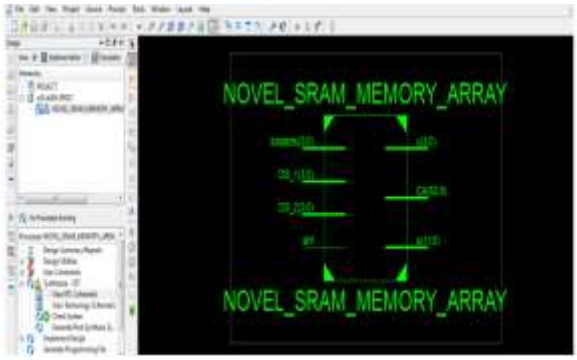

Fig. 2: RTL SCHEMATIC OF PROPOSED SYSTEM

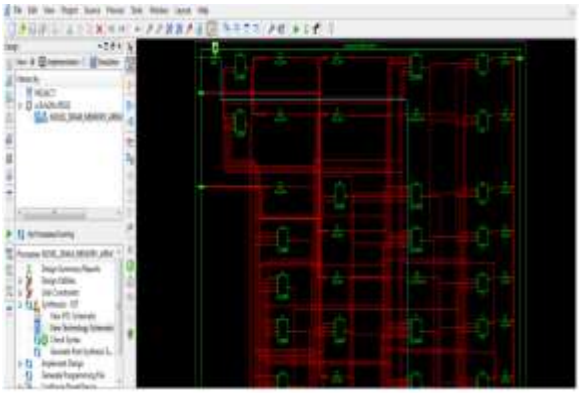

Fig. 3: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM

The Fig. 4 look up table of proposed system. In digital logic, a lookup table (LUT) is a quick approach to realize a complicated function. The value at that address is the capacity yield, and the location is the capacity input. The advantage is that processing the capacity just requires one memory query, which is extremely rapid regardless of how complex the capacity.

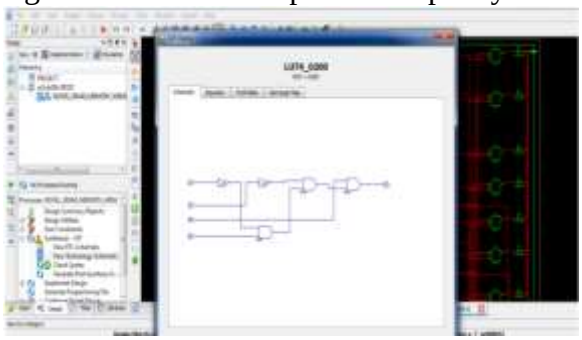

Fig. 4: LOOK UP TABLE OF PROPOSED SYSTEM

The Fig. 5 truth table of proposed system. A reasoning framework's truth table (for instance, a computerized electronic circuit) shows the outputs of the framework for a given input or inputs. A reality table's parts are denoted by inputs and outputs, with the lines addressing all conceivable circuit contributions and the yield comparisons.

Fig. 5: TRUTH TABLE OF PROPOSED SYSTEM

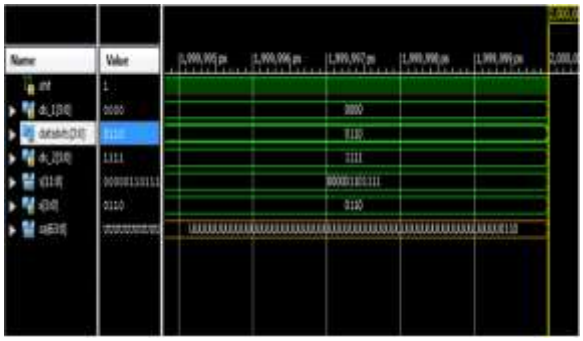

Fig. 6: OUTPUT WAVEFORM OF PROPOSED SYSTEM

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ISSN: 2457-0362

Fig. 7: SYNTHESIS REPORT

V. CONCLUSION

Hence Design and Implementation of Novel SRAM Memory Array with High Security was implemented. Data addresses are decoded by the address control unit using the row and column decoders. There will be read and write operations on this data. Xilinx technology is being used to replicate this. As can be seen from the simulation results, effective output is obtained in terms of latency and area.

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