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ACCURACY -ADAPTIVE SPINTRONIC ADDER FOR IMAGE PROCESSING APPLICATIONS

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ABSTRACT:

Applications involving image processing frequently call for high levels of precision, adaptability, and computational efficiency. The speed and power efficiency of traditional digital adders can be problematic, particularly as data volume and complexity grow. In order to maximize energy consumption, computational speed, and error tolerance, this work proposes an accuracy-adaptive spintronic adder specifically suited for image processing tasks. Utilizing the electron's spin instead of its charge, spintronic devices provide special benefits in terms of scalability and energy efficiency. The suggested adder architecture improves speed and power efficiency for activities with different precision demands by dynamically adjusting its accuracy level based on workload requirements. Because of its versatility, it works well in image processing applications where varied precision and fast data handling are frequently crucial. According to simulation studies, the accuracy-adaptive spintronic adder is a viable option for sophisticated image processing applications since it performs better than conventional digital adders in terms of processing speed and energy economy.

KEYWORDS:

Image processing, spintronic adder,and accuracy-adaptive computing Computational Efficiency, Energy Efficiency, Spintronics, Variable Precision, and High-Speed Computation.

1.INTRODUCTION:

The search for new computing paradigms outside conventional CMOS technology has been fueled by the growing need for fast and energy-efficient computation in contemporary image processing systems. Addition is a key component of many pixel-level operations used in image processing applications such edge detection, filtering, object recognition, and enhancement. Since these applications are frequently used in battery-operated, embedded, or portable systems, maximizing power consumption without sacrificing accuracy and performance has emerged as a crucial design objective. Utilizing the inherent spin and charge of electrons, spintronic devices have become a viable option for next-generation computer systems. These devices have several advantages over their traditional CMOS counterparts, including as fast switching rates, high integration density, ultra-low power consumption, and non-volatility. Specifically, spintronic logic circuits, including adders based on Magnetic Tunnel Junctions (MTJs), have shown promise in lowering energy consumption while

preserving a respectable level of computational performance.

2.LITERATURE SURVEY:

Approximate multipliers based on new approximate compressors by D. Esposito, A. G. M. Strollo, E. Napoli, D. De Caro, and N. Petra

An emerging trend in digital design is approximate computing, which compromises accuracy in processing for speed and power efficiency. In order to construct effective approximation multipliers, this study suggests new approximate compressors and a method to take use of them. Using a 40-nm library and the suggested method, we have created approximation multipliers for a range of operand lengths. The suggested circuits offer superior power or speed for a target precision as compared to previously described approximated multipliers. The research also presents applications to adaptive least mean squares filtering and image filtering.Design methodology to explore hybrid approximate adders for energy-efficient image and video processing accelerators by L. B. Soares, M. M. A. da Rosa, C. M. Diniz, E. A. C. da Costa, and S. Bampi.

In order to investigate the most advanced approximate adders for accelerator architectures developed in the context of multiplier-less multiple constant multiplication optimization problems, this study suggests a novel design methodology. The suggested methodology consists of the following: 1) a search heuristic to find fastest and practical approximate configurations for the architectures being evaluated; 2) low-power techniques regarding hybrid approximate adders design for accelerators based on trees of shift-and-add operations; 3) low-power analysis using the adder optimized by a commercial synthesis tool in the precise part of the approximate adders and high-performance evaluation by exploring parallel prefix adders; and 4) energy efficiency analysis taking into account both the approximate techniques and voltage over scaling estimation. Additionally, enhancements are suggested for the cutting-edge approximate adders that are being assessed.in this document. The Gaussian image filter and the Sobel operator are the two case studies taken into consideration to evaluate the suggested methodology. In relation to the suggested methodology, the exact and approximate image filters were explained using a very high-speed integrated circuit hardware description language. Following synthesis to a 45-nm standard cell-based technology, results are displayed. Taking into account the applications being analyzed, energy reductions ranging from 7.7% to 73.2% were seen for varied quality levels.

Low-power digital signal processing using approximate adders by V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy,In order to precisely calculate the EP and MED of approximate adders for any input pattern at a linear time and space complexity, this research suggests a novel formal approach. According to our experimental findings, the suggested method may compute error-metrics of large approximate adders with accuracy at a speed that is 150 times quicker than Monte Carlo sampling techniques. Next, we create AxMAP, a design tool that generates energy-efficient approximate adders for any given input pattern. It is based on the suggested error-metrics computation. AxMAP generates over 150 distinct adder designs that outperform the current state-of-the-art approximate adders in terms of performance and energy economy when used in image processing applications. A potential strategy for low power integrated circuit design, approximate computing has drawn a lot of research interest lately. In the past, some accuracy-configurable adder designs have been created to support dynamic

levels of approximation. However, because these systems depend on either complex carry prediction or redundant processing, they often have significant area overheads. Some of these designs have circuitry for error detection and repair, which adds even more space. In this study, we examine a straightforward accuracy configurable adder architecture that employs extremely basic carry prediction and without redundancy or error detection/correction circuitry.

A high-performance and energy-efficient FIR adaptive filter using approximate distributed arithmetic circuits by H. Jiang, L. Liu, P. P. Jonker, D. G. Elliott, F. Lombardi, and J. Han

This work proposes an approximate distributed arithmetic (DA) circuit-based fixed-point finite impulse response adaptive filter. Although no multiplication is done explicitly, the radix-8 Booth method is employed in this design to decrease the amount of partial products in the DA architecture. Additionally, the input data is truncated with an error compensation to roughly construct the partial products. An estimated Wallace tree is taken into consideration for the accumulation of partial products in order to further lower hardware expenses. Consequently, the suggested design's latency, area, and power consumption are greatly decreased. Using a 103-tap high-pass and a 48-tap bandpass filter to apply system identification filter demonstrates that the precision of the approximation design is comparable to that of its accurate equivalent. It has a smaller normalized misalignment and a lower steady-state mean squared error when compared to the state-of-the-art adaptive filter that uses bit-level pruning in the adder tree (also known as the delayed least mean square (DLMS) design). According to the synthesis results, the suggested design achieves a 3.2× throughput per area and an average 55% reduction in energy per operation (EPO) when compared to an exact design. Furthermore, when compared to the DLMS design, the suggested design produces an EPO that is 45%–61% lower. The retinal slip of a saccadic system employing the suggested approximate adaptive filter-based cerebellar model is comparable to that of an exact filter. These findings show promise for integrating approximation circuits on a broad scale. into energy-efficient, high-performance systems for applications that are resistant to errors. Significant research has been conducted in the areas of approximation computing and spintronic device technology in recent years due to the increasing need for high-speed, energy-efficient computation in image processing. In image processing applications where small computational errors do not substantially impact visual quality, approximate computing has emerged as a promising design paradigm that permits arithmetic units to forgo a small degree of accuracy in exchange for decreased power consumption, delay, and area. Esposito et al., for instance, suggested new approximation compressors to create effective multipliers with 40-nm technology. Their findings demonstrated significant speed and power gains, and the designs were successfully implemented for adaptive least mean square (LMS) filtering and image filtering, proving usefulness in error-tolerant systems.

3.EXISTING SYSTEM:

We begin by eliminating input "A" from the traditional adder one at a time in order to obtain an approximate adder with fewer input gates. We cannot, however, approach this arbitrarily. In the reduced scheme, the inputs A, B, and Cin do not cause open circuits or short circuits. The resulting simplification should create as few errors as possible in the FA truth table, which

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is another crucial requirement. There is one error in Cout and four errors in Sum in the a forementioned The suggested architecture for an approximate 8-bit adder Since we know that eight-bit addition requires a total of seven full adders and one half adder, we proposed a novel architecture that consists of half adders and full adders.

However, in the suggested method, we suggest a brand-new, innovative 8-bit architecture that allows us to introduce some error on the adder's lsb bit. There is no carry generation unit in this roughly half and full adder. Therefore, we use the proposed approximate half adder on the first LSB bit and one approximate full adder on the second LSB bit. Since there is no carry generate in the third bit, there is no need to use a full adder, so we use a half adder in place of the full adder and then five full adders. As we can see, we can make justice using SPAA matrices and lower the hardware required with minimal error generation.

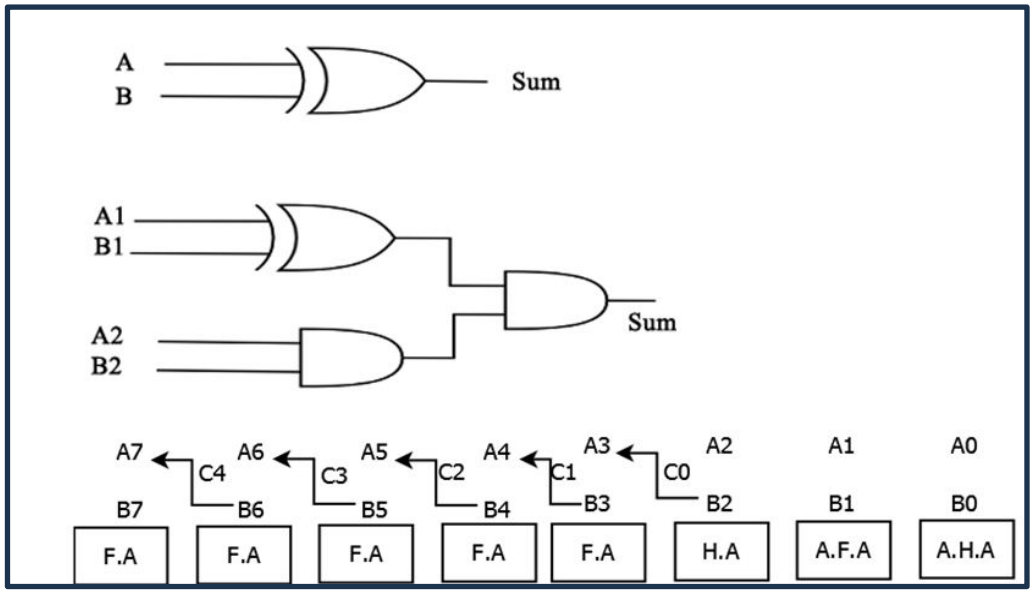

Fig 3: Half Adder using XOR gate,Sum logic using a combination of OR, AND gates

8-bit approximate ripple carry adder

3.1 DESIGN OF MODIFIED ERROR TOLERANT ADDER

In image processing applications and digital signal processing (DSP), the Fast Fourier Transform (FFT) is a crucial function. The computation of FFT involves a very large number of additions and multiplications. As a result, it is an excellent foundation for incorporating cutting-edge techniques like Error Tolerance (ET) into the computational procedure described in this study. While exact results are usually preferable to accurate outcomes in today's VLSI environment, analog integrated circuits (ICs) It is true that not all digital systems can allow the concept of error tolerance; for example, applications involving control systems where the accuracy of output signal is very important and hence the concept of error tolerance cannot be applied; however, there are many examples of applications like DSP applications in which human sensing signals like sight, hearing, touch, and smell are being processed, where we can use this concept. Occasionally, due to its complexity, some novel concepts like error tolerance have emerged. On the basis of this, some designs, such as adders/multipliers, have been

proposed, but they could not perform well in terms of power, speed, accuracy, or area.

Error Tolerant Adder

New ideas and design methods have been put forth in response to the features of digital VLSI design. Among these are the PCMOS technology and the Error Tolerance (ET) concept. A circuit is said to be error tolerant (1) it has a flaw that results in internal and perhaps external faults and (2) the system that uses it generates outcomes that are acceptable. Nonetheless, the 2003 International Technology Roadmap for Semiconductors (ITRS) anticipated the necessity of the error-tolerant circuit.

Necessity of Error Tolerant Adder

The adder is big and quick because of the need for big data sets and quick responses. Because of its poor performance, the traditional Ripple Carry Adder (RCA) cannot be employed. Other adders such the Carry Look Ahead (CLA), Carry Select (CSL), and Carry Skip (CSK) adders exist, but speed and power are always traded off. One possible remedy for this issue is the Error Tolerant Adder (ETA). By further refining the ETA design model, this research lowers the design's cost and chip area.

Adopted Addition Arithmatic

The signal will arrive at the output at a different time after traveling through several paths with uneven delays. Static-0 and static-1 risks, often known as glitches, are introduced by this. Consequently, carry propagation also reduces the adder's speed in a similar manner. Furthermore, faults that occur during this procedure are the primary cause of the high power consumption. Therefore, speed performance and power consumption can be greatly enhanced by avoiding carry propagation. The selected addition arithmetic is displayed in Fig., where S is the output and A and B are inputs. The input operands in this case are separated into two halves. The correct portion, which contains many higher order bits, comes first, followed by the erroneous portion, which contains the Least Significant Bits (LSBs).

Equal length of both portion is not mandatory. Consider for an example, A and B are 16-bits input operands. Here, both operands are split into equal parts for partitioning simplicity. Since higher bits are crucial in determining accuracy, the traditional method of adding the accurate part is done from right to left in order to maintain precision. A unique addition technique is used for the inaccurate component in order to expedite the procedure while using the least amount of electricity possible. The carry propagation path is eliminated with this technique.

The following three steps define the process: (1) From left to right, check each bit position. Conventional 1-bit addition is used if the combination f the two input bits is different from Is.All of the sum bits to the right of the first instance of the input bits "I" are set to "1" regardless of the inputs if both of the input bits are determined to be "1." A = "1011001II0011010" and B = "011010010001011" are two examples to consider. For a typical addition process, this addition should actually produce "100011 lOOlOIOI 101" (72877), but using this method, it produces "100011100100111111" (72863). As a result, TE = 172877 - 72870] = 14 and ACC = (1 - (14/72877)) * 100% = 99.99 % [8] can be used to calculate the Total Error (TE). Consequently, by removing the carry propagation Compared to traditional fast adders, there can be a significant decrease in power usage in the incorrect part.

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4.PROPOSED SYSTEM:

To design our AMFA circuits, let us first look at a baseline (accurate) complete adder in which the outputs (Cout and Sum) may be described by (1) and (2) as functions of the inputs A, B, and Ci

$$C_{out} = A.B + A.C_{in} + B.C_i \quad (1)$$

$$\text{Sum} = A \oplus B \oplus C_i. \quad (2)$$

With the exception of two input combinations, ABCi = "000" and ABCi = "111," the output Sum largely equals the output Cout, according to the truth table of the baseline full adder. There will be two incorrect results out of eight (25% inaccuracy) and an error distance of one if we use the output Cout to estimate the output Sum. Since an incorrect Cout spreads to the subsequent steps and produces more incorrect results, we chose to estimate Sum even though Cout = Sum can be defined.We suggest two new MTJ-based non-volatile approximation 1 bit full adders by estimating the Sum output as Sum = Cout. We also suggest an accuracy-adaptive adder, a complete adder with the special capacity to alter accuracy.

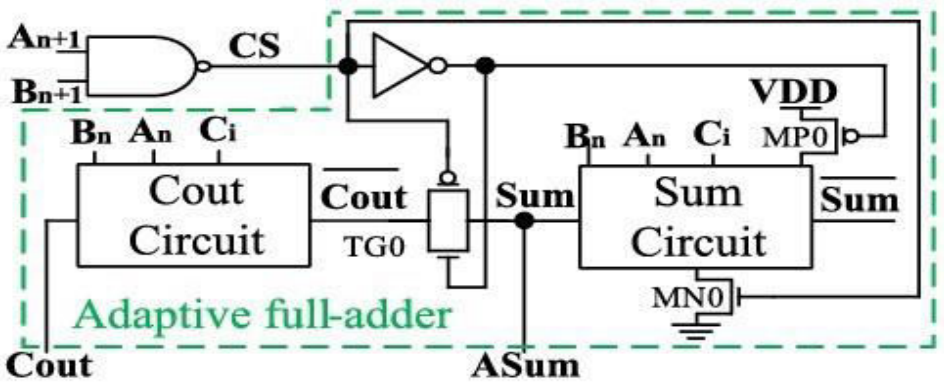

Fig.4.1 shows the proposed sequential AMFA (S-AMFA)

circuit that implements Cout as a majority function by using three parallel MTJs. The pre-charge sense amplifier (PCSA) circuit is coupled to the majority circuit and its complement, which are depicted in Fig. (designated MTJ tree).

The right and the left branches are given in the following equations:

$$R_{\text{Right}} = R_A \parallel R_B \parallel R_{Ci}$$

$$R_{\text{Left}} = R_{\overline{A}} \parallel R_{\overline{B}} \parallel R_{\overline{Ci}}.$$

When the circuit enters the evaluation phase (i.e., Clk goes to logic value “1”), the lower resistance of the right branch discharges the ASum node faster than the Cout node. When the Cout voltage reaches the threshold voltage of the MP1 transistor, it turns on the MP1 transistor and connects Cout to VDD, and the ASum net is discharged to produce the logic value “0.” The left MTJ branch exhibits a lower resistance when there are fewer than two inputs with the

logic value “0.” and makes ASum = "1" and Cout = "0" more quickly. Based on the resistance of the left and right branches, Table I illustrates how the S-AMFA circuit operates.

A PCSA circuit compares the total resistance of the two branches and discharges the associated node with the lower resistance branch. As previously mentioned, the MTJ networks can be implemented by three serial or parallel MTJs. In the serial implementation, the MTJ network's total resistance ranges between 3RAP and 3RP, which is 9× higher than the total resistance of the parallel implementation (with the total resistance of RP/3 to RAP/3). Because the MTJ network with the higher resistance discharges more slowly, the sensing delay increases, causing the proposed S-AMFA to operate more quickly than the MFA.Because the resistance differential between the left and right branches is greater when two complementary reconfigurable MTJ trees are used, read stability is increased and sensing delay is decreased. The suggested S-AMFA would use a comparatively high switching power since MTJ cell reconfiguration uses the majority of energy. We suggest a novel approach, dubbed simplified sequential AMFA (SS-AMFA), that employs both a fixed and a reconfigurable MTJ tree to solve this problem. To reduce the dynamic power consumption of the S-AMFA, we eliminate one of the reconfigurable MTJ branches in SS-AMFA. This results in a little loss of read stability and a slight increase in latency. To put this concept into practice, let's examine the S-AMFA's operation in more detail.

The left branch's equivalent resistance is RAP _ RAP _ RP or higher when the output of the suggested S-AMFA [Fig] changes to "1," whereas the right branch's equivalent resistance is RAP|| RP|| RP or less. As a result, we suggest replacing the MTJ tree. The left branch's equivalent resistance, when at least two SS-AMFA inputs are set to "0," is RP||RP ||RP or RAP || RP ||RP, which is less than the fixed branch's (RP/2) resistance. The node Cout takes the logic value "0" and is discharged more quickly than the node ASum. On the other hand, the left branch's analogous resistance is RAP _ RAP _ RAP or RAP _ RAP _ RAP when at least two inputs are "1."which exceeds the fixed branch's resistance (RP/2). Because it uses fewer reconfigurable MTJs and requires fewer write circuits, the SS-AMFA design notably delivers a greater area efficiency than S-AMFA. Depending on a control signal (CS), expand the S-AMFA and SS-AMFA to operate in "accurate" or "approximate" modes. When the most significant input bits are "1," which indicates that lower order bits do not convey many critical data, this accuracy-adaptive magnetic adder [also known as adaptive AMFA (A-AMFA)] operates in approximate mode.

5.RESULT:

By giving passengers the arrival and departure timings of the bus stops, the bus location indication system aims to enable customers to make precise travel plans. This system was designed using the Arduino UNO. Every bus has an RFID card with a unique ID number on it. The bus stop locations will have entry and exit RFID readers installed. When the bus arrives at the bus stop, the RFID scanner detects the card number, and the arrival time and bus number are recorded in the database. An LCD displays the bus number, arrival time, and departure time. The bus number and arrival and departure times will be inscribed on the SD card. This will guarantee that the data is never destroyed and that the bus records are preserved for a long time. The results of the study show that the RFID-based bus identification system for the blind

effectively increases their sense of independence and confidence. Ninety percent of participants were able to identify the correct bus and its destination using the RFID approach. According to 85% of participants, the method increased their sense of confidence and independence. Eighty percent of participants reported that the method improved their overall experience. These results demonstrate the effectiveness of the system in providing blind people with the information they need to move around freely and safely.

6.CONCLUSION:

Two new non-volatile, low-power AMFAs have been proposed, together with an accuracy-adaptive method for low-power adder design. Power, latency, area, and quality may all be traded off in imprecision-tolerant applications like signal and image processing using the suggested AMFAs. Simulations of image processing demonstrate that considerable power savings (up to 47%) can be achieved at the expense of a little degree of accuracy and quality (19% SSIM reduction and 14% PSNR reduction). Using the proposed parallel MTJ network instead of a serial network in AMFAs may lead to a 94% reduction in propagation delay compared to earlier non-volatile MFAs. When compared to conventional AMFAs, the adaptive techniques suggested in this article result in significant PSNR and SSIM at the expense of a small area and power overhead. Improvements in accuracy (26% error rate and 74% NED) and accuracy (11% and 19%) are possible. In order to further reduce leakage current and standby power, the circuit's full non-volatility feature also enables it to shut down fully during idle modes without causing data loss or requiring any additional components for state backup or recovery.

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