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DESIGN OF LOW POWER HAMMING CODE - ENCODING, DECODING AND CORRECTING CIRCUITS BY USING REVERSIBLE LOGIC

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ABSTRACT: An ideal communication relies on error detection and correction techniques for faultless data transmission. Hamming code is widely known among those techniques for single bit error detection and correction capacity. Low power circuit design yields many favorable conditions like increased performance, system capacity, minimized cost etc. Reversible logic is an excellent approach to optimize heat dissipation and information loss. As Hamming code is designed using irreversible logic gates there is undesired power dissipation. So, to improvise this downside, this paper elucidates the design of low power Hamming code using reversible logic gates which detects and corrects errors if any. The power dissipation for the proposed design is 7.2µW when the power of individual components is added theoretically. The overall power of the circuit is 5.8µW.The mathematical analysis of quantum cost calculation, garbage outputs, delay and area is presented in this paper. Finally, simulation and synthesis results are attained by using Xilinx ISE 14.4.

KEYWORDS: Hamming code, error detection and correction techniques, Reversible logic and Xilinx.

I. INTRODUCTION

Digital data transmission is the base of all modern-day applications. During its way from the transmitter to receiver, errors are induced to data due to noise and environmental interferences. An error occurs when a bit is altered between transmitter and receiver. To eliminate these errors, error detection and error correction circuits are built into all digital circuits. Error correction adds redundancy bits to the existing data to make the data transmission resistant to external disturbances [1].

Hamming code is a set of error correction codes that can be used to detect and correct bit errors that occur when computer data is moved or stored. Hamming code makes use of concept of parity and parity bits, which are bits added to data so that the validity of the data can be checked when it is read or after it has been received in a data transmission [2].

Parity involves counting the number of ones in a unit of data, and adding either a zero or one (called parity bit) to make the count odd (for odd parity) or even (for even parity).

- To calculate even parity "XOR" operator is used.
- To calculate odd parity "XNOR" operator is used.

Parity bits occupy the position of $2^0, 2^1, 2^2, \ldots\ldots\ldots\ldots 2^n$.

Hamming code circuit, when constructed using conventional irreversible gates, dissipates a huge amount of power. Power consumption is the primary consideration in any circuit designing. Hence, the irreversible gates are replaced with reversible gates, thereby reducing the overall power consumption of the circuit. Various error detection and correction codes are in existence such as parity checking, cyclic redundancy check, etc [3]. Hamming code is the most commonly used error

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checking and error correction code as it is easy to implement. It adds limited redundancy bits to the data, keeping the code simple. However, Hamming code is a single error correcting code. It can be used only when the error rate is low. There are different types of reversible logic gates are available which is used to perform some functions are operations same like irreversible logic gates (and, or, xor, xnor). But the main advantage of designing the circuits using RG gates is that the circuit dissipates no heat, increase the performance, decrease in delay, power consumption which are main requirements in VLSI circuits [4].

II. EXISTED DESIGN

Hamming code encoding and decoding circuits are implemented using conventional irreversible logic gates. To perform error detection, the circuit adds one or more extra bits called parity bits to the existing information bits while transmission of data. This is called encoding. Decoding involves calculation of check bits which is illustrated in the existing work. These check bits help to detect and correct the error. (7, 4) Hamming Code gives out 7- bit code by encoding 4 data bits by adding 3 parity bits. With these parity bits, it can not only detect single bit error but it can also correct them.

Encoder Circuit: Data word is applied as an input in the encoder circuit which performs XOR operations on the given data word and thus the required parity bits are generated from the parity generator. Parity bits and data bits together form the code word. An encoder circuit of hamming code for 4 bit data word is shown below.

Decoder Circuit: In the decoder circuit, code word is applied as input. Then check bits are generated by the checker bit generator to check the parity bits. These check a bit locates the error in the code word by means of decoder circuit. The Output of decoder enables a demultiplexer which is connected to the input code words. If no error occurs then the select line of demultiplexer flows the input form line I0 and the I1 is set to logic '1'. So from the logic OR gate we can obtain the data. Now if errors occur then the select line of the demultiplexer flows the code word from line I1 and I0 is set to logic '0'. Thus inverting the bits, the error bit is corrected and thus we can obtain the error free data. A decoder circuit of hamming code for 4 bit data word is also shown below.

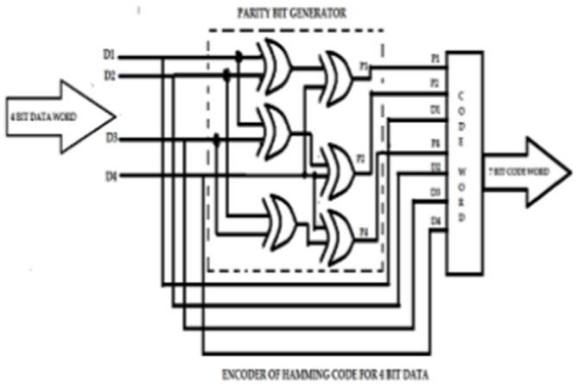

Fig. 1: ENCODER CIRCUIT OF HAMMING CODE FOR 4BIT DATA

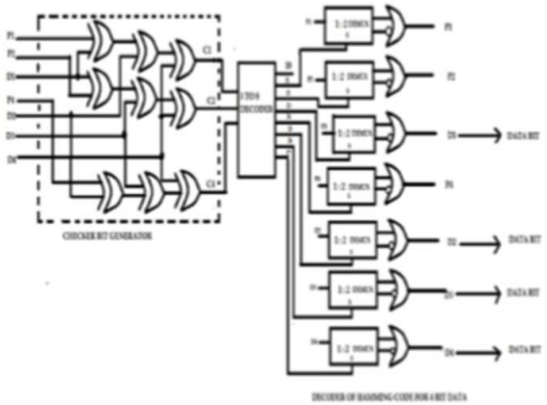

Fig. 2: DECODER CIRCUIT OF HAMMING CODE FOR 4BIT DATA

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V. Shiva Prasad Nayak, Govind Prasad, K. Dedeepya Chowdary and K. Manjunatha Chari, "Design of Compact and Low Power Reversible Comparator" [5], According to the Launder's principle, in binary for each bit loss information kTln2 of heat is dissipated. All the present designs like CMOS are irreversible logics which losses bit information. Reversible logic is the better way of reducing power consumption. Bit loss always give the more power consumption but here by recovering bit loss using reversible logic we are getting less power consumption, as well as less number of gates and high speed. In this paper, we proposed a reversible n-bit binary comparator, the calculation for quantum cost, number of gates, garbage outputs, power, delay and algorithm for constructing is presented.

Debalina Roy Choudhury, Krishanu Podder, "Design of Hamming Code Encoding and Decoding Circuit Using Transmission Gate Logic" [6]. The Hamming code encoder and decoder circuit is implemented using transmission gate logic. The architecture is simulated with different technologies (16nm, 22nm, 32nm, and 45nm) with the help of TANNER EDA Tool for the study of total power dissipation of the circuit. The analysis shows that with the decrease of channel length, there is an decrease of 12.65 % and 2.37 % power dissipation in 16nm compared to 22nm in encoder and decoder circuit. The values of model parameters are used from Predictive Technology Model (PTM). For circuit verification, the hamming code algorithm is implemented in Spartan 3A family XC3S700A FPGA device using VHDL coding technique.

III. PROPOSED SYSTEM

Power optimized hamming code encoding and decoding circuits using reversible logic for detection and correction of single bit errors. This paper designed three reversible blocks, one to encode the existingdata by adding parity bits. The second block generates check bits. These check bits aid in error detection. If any error is introduced to the code word during the transmission process, the third block detects and decodes the check bits, finds out the faulty bit and corrects it, thereby giving final error free output. Each of the above circuitry is explained as follows.

3.1 EC Reversible Logic Cell

EC is constructed using three F2G gates and two FG gates. EC has low quantum cost and zero garbage outputs thereby enhancing the power consumption of the circuit. It has four inputs and seven outputs. The four inputs are data bits. EC cell calculates parity bits for the given data. The parity bits are placed in the places that are numbered in powers of 2. The parity bits are calculated using the algorithm. The output of FG and F2G gates is simply XOR operation of the given inputs. The output is 7-bit code word with four data bits and three parity bits.

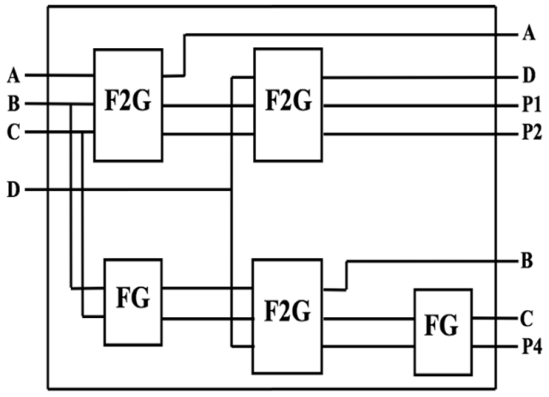

Fig. 3: EC LOGIC CELL ARCHITECTURE

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3.2 CG Reversible Logic Cell

To check if the bit stream has reached safely to the destination, check bits are calculated at the receiver end. CG calculates check bits using the algorithm suggested in [4]. If an error is present, the error position is located by observing check bits. $C_4C_2C_1$ gives the position of the error in binary.

To construct CG, two F2G gates and five FG gates are used. The output of EC is considered as input to CG. CG has encoded word as input and three outputs i.e., check bits. Fig.2 shows the construction of CG Reversible Logic cell.

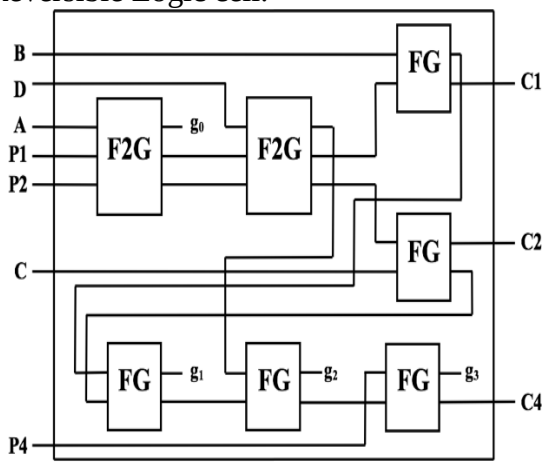

Fig. 4: CG LOGIC CELL ARCHITECTURE

3.3 Proposed EDC Reversible Logic Cell

By now, the error position has been determined. To correct the bit, we must invert the bit located in the position $C_4C_2C_1$. This is done using EDC cell. It consists of a decoder which takes $C_4C_2C_1$as input and identifies the position of the error. The decoder has been implemented using Fredkin gates. The FG gates at the end act as EXOR gates. EXOR gate acts as an inverter when the second input is given as 1. Therefore, after locating the error position, the corresponding FG gate inverts the bit in the error position giving us corrected output. CG is cascaded with EDC cell to obtain proposed circuit. EDC cell consists of a decoder and seven EXOR gates implemented using reversible logic. Fig. 3 explains detail schematic of EDC. Simulation results are analyzed in section 4 to test the proposed circuit.

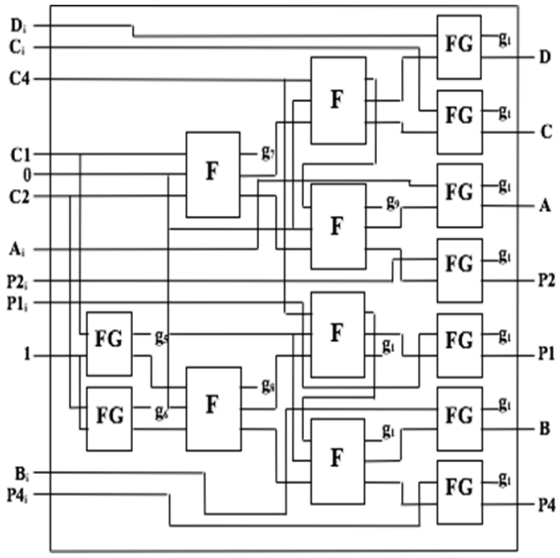

Fig. 5: EDC LOGIC CELL ARCHITECTURE

IV. RESULTS

The corresponding simulation results of propose hamming code encoding, decoding and correction circuits using reversible logic is shown below. Inputs a, b, c, d are supplied from test bench we can apply any number of inputs and can observe the respective output to verify whether the design is working properly or not.

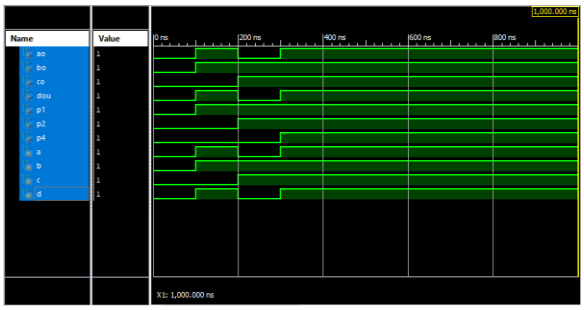

Fig. 6: SIMULATION OUTPUT OF PROPOSED EC USING REVERSIBLE LOGIC GATES

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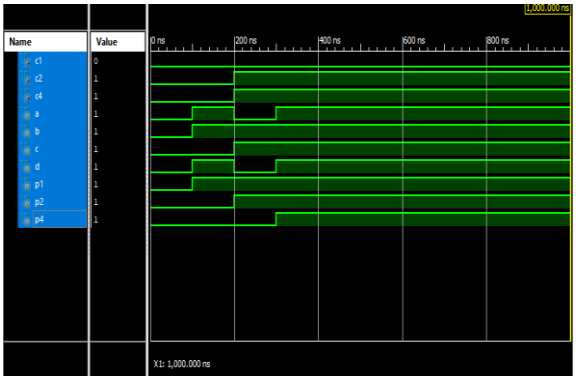

Fig. 7: SIMULATION OUTPUT OF PROPOSED CG USING REVERSIBLE LOGIC GATES

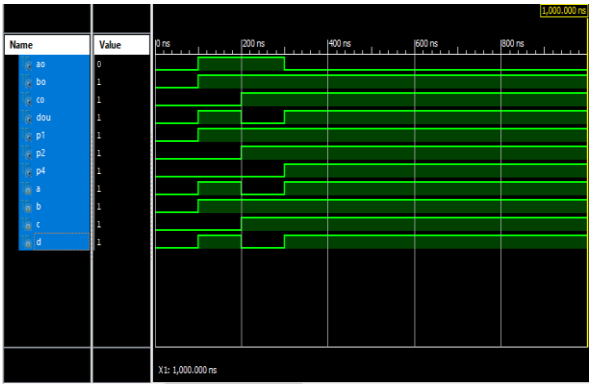

Fig. 8: SIMULATION OUTPUT OF PROPOSED EDC USING REVERSIBLE LOGIC GATES

V. CONCLUSION

This paper provides an innovative approach to reduce power consumption in irreversible hamming code circuitry using reversible logic gates. As hamming code is designed using irreversible logic gates, there is undesired power dissipation. So, to improvise this downside, the design of low power hamming code using reversible logic gates which detects and corrects the error if any. Proposed reversible Hamming Code encoding and decoding circuit have 27 number of gates and power consumption is 7.2mW. Number of gates, Quantum cost, Garbage output and delay are 27, 39, 18 and 1ns respectively.

VI. REFERENCES

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