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HYBRID FLIP-FLOP WITH CONDITIONAL BOOSTING FOR NEAR-THRESHOLD VOLTAGE MANAGEMENT

[1]Dr. G. Jyoshna, [2]G. Lavanya

Assistant Professor, ECE Department, Sri Krishnadevara University College of Engineering and Technology (SKUCET), Ananthapur, Andhra Pradesh.

Department of ECE, Sri Krishnadevara University College of Engineering and Technology (SKUCET), Ananthapur, Andhra Pradesh.

Abstract: For an ultralow voltage application, when the supply voltage is lowered to the vicinity of the threshold, a conditional-boosting flip-flop is suggested. In order to provide minimal latency and less performance fluctuation in the near-threshold voltage area, the suggested flip-flop uses voltage boosting. In order to reduce switching power usage by doing away with unnecessary boosting operations, it also uses conditional capture. In comparison to conventional precharged differential flip-flops, the suggested flip-flop offered up to 72% lower latency with 75% less performance variability due to process variation and up to 67% improved energy-delay product at 25% switching activity, according to experimental results in a 65-nm CMOS process.

Index Terms: near-threshold, flip-flops, and bootstrapping.

1. INTRODUCTION

Energy-efficient computing is necessary for portable electronics to have a long operating life on a small power budget. One efficient method for reducing the power consumption of CMOS digital circuitry is voltage scaling [1]. Regrettably, considerable speed deterioration results from aggressive voltage scaling, such in subthreshold computing.

It seems that near-threshold computing is a workable way to reduce energy consumption while taking delay into account [2]. However, in many applications that need fast speed and low power, the still increased latency and performance unpredictability of circuits operating in the nearthreshold voltage region may be undesirable. For instance, performance parameters like latency, setup time, and hold time will be severely impacted if clocked timing elements like latches and flip-flops—which are important circuit components in high-speed synchronous systems—are operated in the near-

threshold region. This will have an unfavourable impact on the overall performance of the system. The issues brought on by aggressive voltage scaling may be resolved by capacitive boosting [8]–[10]. It permits certain MOS transistors to have their gatesource voltage raised above or below the supply voltage. The resultant improved driving capacity of transistors may lower latency and lessen its susceptibility to changes in the process. This method is used by the bootstrapped CMOS driver described in [8] to drive large capacitive loads with much lower latency. But since it's a static driver, the bootstrapping process is triggered by each input transition. To reduce redundant power usage, the conditional bootstrapping idea is proposed by the conditional-bootstrapping latched CMOS driver [9]. Because it is a latched driver, it can only permit boosting in situations when the logic values of the input and output disagree. This eliminates redundant boosting and improves energy economy, particularly when there is little switching. For quick operation in the near-threshold voltage range, a differential CMOS logic family that adapts the boosting approach has also recently been developed [10].

2. CONCEPT OF PROPOSED FLIP-FLOP FOR CONDITIONAL BOOSTING

There are four possible input data capture scenarios that need to be taken into consideration in order to include conditional boosting into a precharged differential flip-flop. These scenarios are based on the logic states of the input and output. The following are these scenarios:

1) A high input should cause boosting to occur for a quick capture of incoming data if the output is low;

2) A low input should cause boosting to occur if the output is high since the input does not need to be captured;

3) A high input should cause boosting to occur for a quick capture of incoming data if it is low;

4) A high output should cause a high input to cause no boosting.

By combining two operating principles, these possibilities may be implemented into a circuit design using a single boosting capacitor. One is that the data stored at the output (also known as output-dependent presetting) must be used to establish the voltage presetting for the boosting capacitor's terminals. The flip-flop's input data must provide the conditional basis for

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boosting operations (also known as input-dependent boosting). Fig. 1 displays the conceptual circuit diagrams that serve as evidence for these ideas.

As shown in Fig. 1(a), outputs Q and QB are used to calculate the preset voltages of capacitor terminals N and NB in order to facilitate output-dependent presetting. The noninverting input (D) is coupled to NB through a nMOS transistor, and the inverting input (DB) is coupled to N through another nMOS transistor, as shown in Fig. 1(b). To support the inputdependent boosting, N and NB are preset to be high and low if Q and QB are high and low, and low and high if Q and QB are low and high, respectively, [left diagram in Fig. 1(a)]. Next, in one scenario where the flip-flop stores low data, which causes the capacitor to preset as shown in the left diagram in Figure 1(a), a high input causes NB to be pulled to the ground, allowing N to be boosted towards –VDD as a result of capacitive coupling [upper left diagram in Figure 1(b)]. N may be connected to the ground in the meanwhile thanks to a low input, but since the node is already set to VSS, there is no voltage change at NB, therefore there is no boosting [bottom left schematic in Fig. 1(b)]. A low input enables N to be dragged down to the ground, allowing NB to be boosted towards − VDD due to capacitive coupling [lower right diagram in Fig. 1(b)], similar to the opposite situation in which a high data is stored in the flip-flop, resulting in the capacitor presetting described in right diagram in Fig. 1(a).

Although the node is already set to VSS, a high input permits NB to be connected to the ground; nevertheless, this prevents any voltage change at N, which prevents boosting [upper right schematic in Fig. 1(b)].

To make these procedures simpler to grasp, Table I summarises them. These actions enable the removal of any unnecessary boosting, which significantly reduces power consumption, particularly when switching activity is minimal.

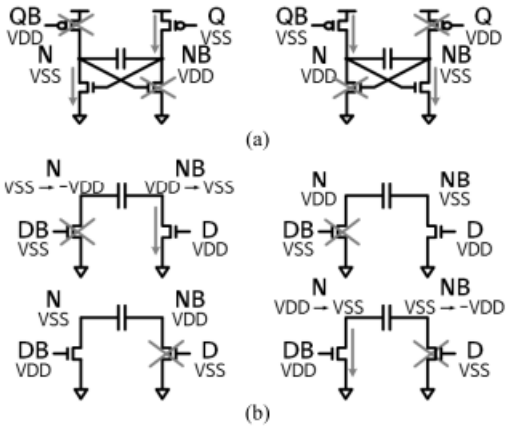

Fig. 1. Conceptual circuit diagrams for (a) output data-dependent presetting and (b) input data-dependent boosting

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3. CIRCUIT IMPLEMENTATION

Fig. 2 illustrates the suggested conditional-boosting flip-flop (CBFF) structure, which is based on the ideas covered in the preceding section. It is made up of an explicit short pulse generator, a symmetric latch, and a conditional-boosting differential stage. The input-dependent boosting in the conditional boosting differential stage shown in Fig. 2(a) is carried out by MN5/MN6/MN7 with boosting capacitor CBOOT, while the output-dependent presetting is carried out by MP5/MP6/MP7 and MN8/MN9. The symmetric latch is represented by MP8–MP13 and MN10–MN15 in Fig. 2(b).

Figure 2(c) illustrates a unique explicit pulse generator that generates a short pulsed signal PS that drives certain transistors in the differential stage. The suggested pulse generator, in contrast to traditional pulse generators, lacks a pMOS keeper, which allows for faster speed and reduced power consumption because there is no signal fighting while the PSB is being pulled down. In addition to assisting in a quick pull-down of PSB, MP1 inserted in tandem with MN1 plays the job of the keeper in maintaining a high logic value of PSB.

MN1, MP1, and I1 quickly discharge PSB at the CLK's rising edge, allowing PS to rise. Following I2 and I3 delay, MP2 charges PSB, causing PS to go back to low. This causes a short positive pulse at PS, the width of which is influenced by I2 and I3 latency. MP1 keeps PSB high when CLK is low while MP2 is turned off.

Based on our analysis, the energy savings may reach 9% while maintaining the same slew rate and pulsewidth.

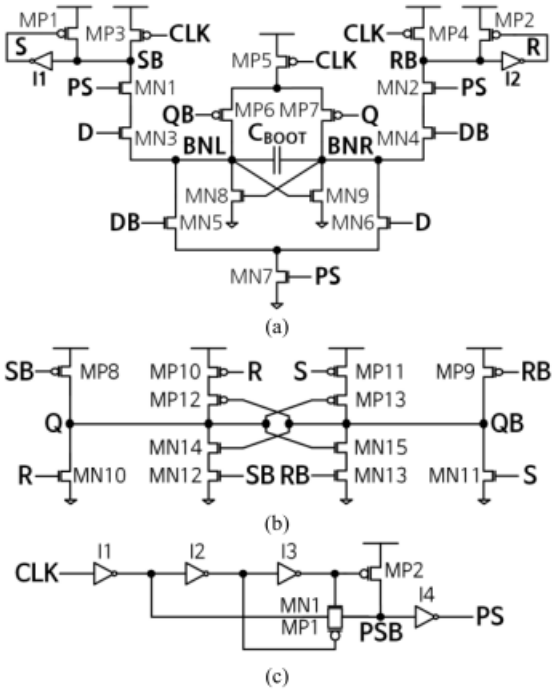

Fig. 2. Proposed CBFF. (a) Conditional-boosting differential stage. (b) Symmetric latch. (c) Explicit brief pulse generator.

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4. SIMULATED AND MEASURED RESULTS

The suggested CBFF and other flip-flops, including the adaptive-coupling flip-flop (ACFF) [6, the sense amplifier-based flip-flop (SAFF) [3, the differential skew tolerant flip-flop (STFF-D) [4, the static contention-free single-phase-clocked flip-flop (SCFF) [5, and completely. In a 65-nm CMOS process, static topologically-compressed flip-flops (TCFFs) [7] are constructed and assessed. A single explicit pulse generator is shared by four primary flip-flop circuits in the proposed flip-flop with shared pulse generator (CBFF-SP), which is also developed and compared. Every flip-flop has a device size that is specifically designed to reduce EDP at every supply voltage. A 15 fF capacitive load is connected to each flip-flop's output.

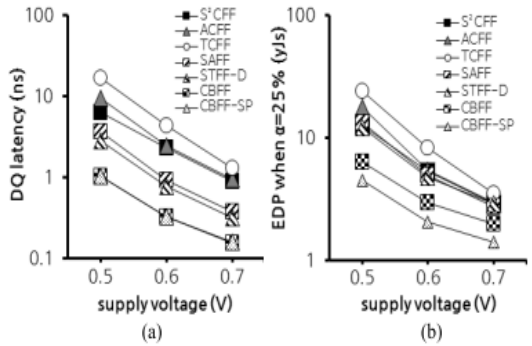

Fig. 3. Simulation results at various supply voltages. (a) DQ latency. (b) EDP.

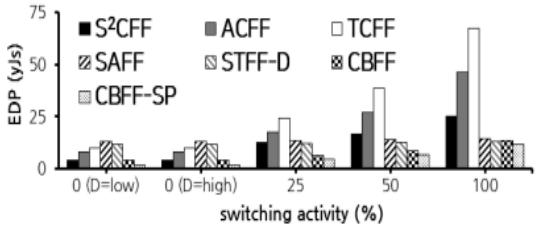

Fig. 4. Simulated EDP at various switching activity conditions at 0.5 V.

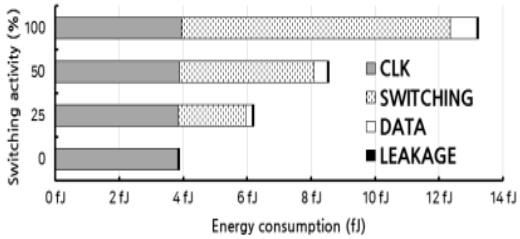

Fig. 5. Simulated energy of CBFF at 0.5 V with various switching activities.

The boosting capacitor is implemented using a MOM capacitor. The suggested flip-flop's pulse width is chosen to provide sufficient margins to ensure data collection even in the most dire circumstances. The energy-delay product (EDP) and simulated data-to-output (DQ) latency of flip-flops at supply voltages between 0.5 and 0.7 V. As, at 25% switching activity, CBFF outperforms SAFF and STFF-D by up to 72% and 63%, respectively, and has up to 53% and 47% lower EDPs. By sharing a pulse generator across many flip-flops, CBFFSP also has up to 67% and 63% lower EDPs [Fig. 5(b)] than SAFF and STFF-D as well.

Due to their significantly high DQ latency, S2CFF, ACFF, and TCFF perform worse in terms of EDP. The simulated EDP of flip-flops at 0.5 V supply voltage in accordance with input switching activity. Because of conditional operation, the EDP improvements of CBFF and CBFF-SP over SAFF are as high as 70% and 85%, respectively. breaks down the power consumption of the suggested flipflop into its component parts, demonstrating how the switching power component reduces as switching activity does. to the boosting conditional. When switching is at zero, the clock circuit—which includes the pulse generator—consumes the bulk of the power. When the DQ latencies of flip-flops are compared with random process variation using a 1000-point Monte Carlo simulation, it becomes clear that the DQ latencies of CBFF and CBFF-SP are very resistant to process changes in the near-threshold voltage range. More specifically, compared to SAFF and STFF-D, CBFF has a DQ latency standard deviation that is 75% and 85% lower, respectively. Additionally, compared to SAFF and STFF-D, CBFF-SP has an EDP standard deviation that is 67% and 87% lower, respectively. We summarise the flipflop performance in Table II. The suggested flip-flops take up more layout space and need more gadgets. Since S2CFF, ACFF, and TCFF are designed to be low power, their EDP performance is poor due to their high DQ latency and tiny energy consumption. Due to its pulsed operation, the suggested flip-flop has a comparatively long hold time; buffer stages at the output may be necessary to prevent hold time violations. Our analysis shows that buffer stages, which are used to prevent this problem, result in an approximate 7% EDP cost at 25% switching activity.

5. CONCLUSION

A new CBFF has been presented for aggressive voltage scaling down to the near-threshold voltage range without significant performance compromise. The suggested flip-flop has less DQ latency, lower EDP, and less sensitive to process variation, according to the assessment in a 65-nm CMOS process.

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AUTHORS

1. Dr. G. Jyoshna, Assistant Professor, ECE Department, Sri Krishnadevara University College of Engineering and Technology (SKUCET), Ananthapur, Andhra Pradesh, Pin: 515003, Email: girikajyoshna@gmail.com

2. G. Lavanya, Department of ECE, Sri Krishnadevara University College of Engineering and Technology(SKUCET),

Ananthapur, Andhra Pradesh, Pin:515003,
Email: gangasanilavaya@gmail.com