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Ladner Fischer Adder

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ABSTRACT

A parallel-prefix adder gives the best performance in VLSI design. However, performance of Ladner-Fischeradderthroughblackcelltakes hugememory.So,graycell canbe replacedinsteadof blackcellwhichgivestheEfficiency in Ladner-Fischer Adder. The proposed system consists of three stages of operations they are pre-processing stage, carry generation stage, post-processing stage. The pre-processing stage focuses on propagateand generate, carry generation stage focuses on carry generation and post-processing stage focuses on finalresult. In ripple carry adder each bit of addition operation is waited for the previous bit addition operation. Inefficient Ladner - Fischer adder, addition operation does not wait for previous bit addition operation andmodification is done at gate level to improve the speed and to decreases the memory used. General TermsRipplecarry adder, Efficient Ladner–Fischer adder,Black cell, Gray cell.

1. INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs)and hence increasing theirspeedandreducingtheir power/energyconsumptionstronglyaffectthe speedandpower consumptionofprocessors. There are many works on the subject of optimizing the speed and power of these units, which havebeenlow-power/energy consumptions,which isa challengefor thedesigners ofgeneralpurposeprocessors.

One of the effective techniques to lower the power consumption of digital circuits is to reduce the supplyvoltageduetoquadraticdependenceoftheswitchingenergyonthevoltage.Moreover,thesubthresholdcurrent,which isthe main leakage component in OFF devices, has an exponential dependence on the supply voltagelevelthroughthedrain-inducedbarrierloweringeffect.Dependingontheamountofthesupplyvoltagereduction,theoperationofONdevicesmayresideinthesuperthreshold,near-threshold,orsubthresholdregions.Workingin the super threshold region provides us with lower delay and higher switching and leakage powers comparedwiththenear/sub threshold regions.

In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences onthesupplyandthresholdvoltages.Moreover,these voltagesare(potentially)subjecttoprocessandenvironmentalvariations in the nano scale technologies. The variations increase uncertainties in the aforesaid performanceparameters. In addition, the small sub threshold current causes a large delay for the circuits operating in the subthreshold region . Recently, the near-threshold region has been considered as a region that provides a moredesirable trade offpoint between delay and power dissipation compared with that of the sub threshold one,because it results in lower delay compared with the sub threshold region and significantly lowers switching andleakage powers

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compared with the super threshold region. In addition, near-threshold operation, which usessupply voltage levels near the threshold voltage of transistors, suffers considerably less from the process andenvironmentalvariations compared with thesub threshold region.

Thedependenceofthepower(andperformance)onthesupplyvoltagehasbeenthemotivationforde signof circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energyconsumption,thesystemmaychangethevoltage(andfrequency)ofthecircuitbasedontheworkload requirement.Forthesesystems,thecircuit shouldbeabletooperate under awiderangeof supplyvoltagelevels.Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adder as onethemain components, could becrucial in thedesignof high-speed, yet energy efficient,processors.

Inadditiontotheknobofthesupplyvoltage,on emaychoosebetweendifferentadderstructures/fami liesfor optimizing power and speed. There are many adder families with different delays, power consumptions, andareausages.Examplesincludecarrysaveadder(CSA),carryskipadder(CSKA),andcarryselectadder(CSLA).

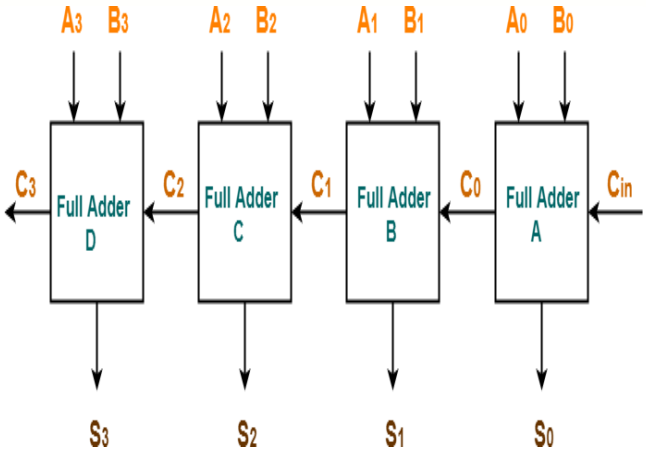

Fig1.14bit ripplecarry adder

Thedescriptionsofeachoftheseadderarchitecturesalongwiththeircharacteristicsmaybefoundinand.TheRCAhasthesimplestructurewiththesmallestareaandpowerconsumptionbutwiththeworstcriticalpathdelay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of theRCA. The PPAs, which are also called carry save adder, exploit direct parallel prefix structures to generate thecarryas fast as possible.

There are different types of the parallel prefix algorithms that lead to different PPA structures withdifferent performances. As an example, the carry save adder (CSA) is one of the fastest structures but results inlargepowerconsumptionandareausage.Itshouldbenotedthatthestructurecomplexitiesof PPAsaremorethanthose of other adder schemes. The CSKA, which is an efficient adder in terms of power consumption and areausage,wasintroducedin.Thecriticalpathdelayoftheis muchsmallerthantheoneintheRCA,whereasits area and power consumption are similar to those of the RCA. In addition, the power-delay product (PDP) oftheCSKAis smallerthan thoseof theCSLAand PPA structures.

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Inaddition,duetothesmallnumberoftransistors,the CSKAbenefitsfromrelativelyshortwiringlengthsas wellas a regular and simple layout. The comparatively lower speed of this adder structure, however, limits its use forhigh-speed applications. In this paper, given the attractive features of the CSKA structure, we have focused onreducingits delay by modifying its implementation based onthe static CMOS logic.

TheconcentrationonthestaticCMOSorigina tesfromthedesiretohaveareliablyoperatingcircuitu ndera wide range of supply voltages in highly scaled technologies. The proposed modification increases the speedconsiderably while maintaining the low area and power consumption features of the CSKA. In addition, anadjustmentofthestructure,basedonthevariablelat encytechnique,whichinturnlowersthepowerconsu mptionwithout considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no workconcentrating on design of CSKAs operating from the super threshold region down to near-threshold region andalso, the design of (hybrid) variable latency CSKA structures have been reported in the literature. Hence, thecontributionsof this paper can besummarizedas follows.

1) Proposing a modified CSA,CSLA and CSKA structure by combining the concatenation and the incriminationschemestotheconventionalCSA,CSL AandCSKA(Conv-CSKA)structureforenhancingthespeedandenergye fficiencyoftheadder.Themodificationprovidesusw iththeabilitytousesimplercarryskiplogicsbasedont heAOI/OAIcompound gates instead of themultiplexer.

2) Providingadesignstrategyforconstructinganeffi cientCSA,CSLAandCSKAstructurebasedonanalyt icallyexpressionspresented forthe critical path delay.

Informationlossandenergydissipationarethemajor problemsfacedinthepresent-daytechnology.Theproblemcan be rectified using reversible logic. The reversible gate consists of equal number of outputs and inputs. It alsohas one to one correspondence between output and input ports. The operation of the circuit is backwards so thatthe inputs can be easily retrieved from the outputs. And they can be stopped and go back at any point during thetime of computation. The conventional gates like XOR, OR, AND which are used in construction of a digitalcircuits will not perform reversible operations, this leads to information loss which produces dissipation of heat.The loss of information for every bit, generates heat which is given by formula KT*log2 Joules where K is theBoltzmann‟s constant and T is the Absolute Temperature. The demand for reversible circuits is more in VLSIdesign because there is no information loss and it dissipates zero heat. So, it provides low power consumptionwhiledesigningcomplexVLSIcircuits .FouraddercircuitsaredesignedusingReversibleLo gicGates.TheyaredesignedusingSMG,Feynmanan dFredkingates.Thefirstdesignistheimplementation offour-bitAdder/Subtractor(Ripple)usingreversiblegates whichwillgeneratefour-bitSumandaCarry.Forimplementingfour-bit reversible ripple carry adder, four Feynman gates and four SSS gates are utilized. It can be used as bothAdder and Subtractor. The operation mechanism can be done by using XOR gate. The Feynman Gate will act asXOR gate in Reversible Logics. The second circuit is the design of Carry

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Skip Adder using reversible logic. TheCarry Skip Adder is constructed with SMG gate and Fredkin gate. Three Fredkin gates are used to perform theAND operation to compute propagate signal. Single Fredkin gate is used to compute the AND-OR logic whichwill generate the carry out signal. The third design is the implementation of Carry Select Adder using reversiblelogic gates like SMG gate and Fredkin gates. This is the fastest of all adders available which is used in manyapplications like processors to compute Arithmetic operations. It performs two addition operations in parallel.Two Four-bit ripple carry adders designed using SMG gate and five modified Fredkin gates are used to generatethe Carry and Sum for the four-bit carry select adder. The fourth design is the implementation of Carry SaveAdderusingReversibleLogic.PeresgateandSMGgatesareusedtogenerateSumandCarry.InreversibleCarrySave Adder, all the full adders blocks are replaced by newly proposed SMG gates. It is arranged in a binary treestructure.Thetotal sum is generatedby moving the carry sequenceto its left sidebyoneunit.

In this process the reversible computation can be done to some extent. It uses deterministic transitions from onestatetoanotherstate.Anobligatoryconditionforreversibilityistherelationbetweentheinputsandoutputsof non-zero probability to their substitute inputs must be similar to their outputs. It is in the form of unconventionalcomputing[1-2].Themostcloselyrelatedtypesof reversiblecomputingisbasedonthephysicalperformanceofthedevice and the logicalperformanceof thedevice.

Addition operation is the main operation in digital signal processing and control systems. The fast and accuracyof a processor or system depends on the adder performance. In general purpose processors and DSP processorsthe addition operation addresses are taken from simple ripple carry adder [1] . Ripple carry adder is used for theadditionoperationi.e.,ifNbitsadditionoperationisperformedbytheN-bitfulladder.Inripplecarryaddereachbit full adder operation consists of sum and carry, that carry will be given to next bit full adder operation, thatprocess is continuous till the Nth bit operation. The N-1 th bit full adder operation carry will be given to the N thbit full adder operation present in the ripple carry adder. For 16-bit ripple carry adder, the first bit carry is givento second bit full adder, second bit carry is given to the third bit full adder, similarly the operation is continue tillfifteenth bit carry is given to sixteenth bit full adder. The addition operation is performed from least significantbittomostsignificantbitinripple carryadder.Configurationlogicandroutingresourcesin FieldProgrammableGateArray.

2.LITERATURESURVEY

Intheyear1973,thescientistC.H.BENNETTdescribesacomputationwhichiscarriedinReversiblelogicwhichproduce no heat dissipation. Because the amount of energy dissipated in entire block is directly proportional tothenumberofbitserasedduringtheprocessofthecomputation.Ifthecircuitisdesignedinsuchawaythatthereis no information loss then it is called as reversible which is mentioned in [2]. Reversible circuits are designedusingreversiblelogicgates.Reversiblegatewillproduceuniqueoutputvectorforeachsetofinputvectorappliedanditisviceversaonly.Withthehelpofquantumprimitivegates,anewreversiblegateisdesign

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ed.Thedesignednew gates will have a ability to produce all conventional logical operations like AND, NAND, OR, NOR, XOR,XNOR. The design of the full adder is made by using newly proposed SMG Gate. The newly proposed gate ismore efficient than the other full adder circuits constructed by Toffoli, Feynman gates and Peres gate [8]. Thescientist Landauer explains that both logical irreversibility and physical irreversibility are closely associated andthey require a minimum heat generation for every cycle performed. For each bit of information lost producesk*T*log2Joulesofenergy,wherekisBoltzmann‟sconstantandTtheabsolutetemperaturewheretheoperationsarebeingperformed.Toperformsomecomputationsinconventionalsystemsomemillionsoftransistorsareused.Author[1]provesthattherewillbenodissipationofheatifblocksarereplacedwithreversiblecircuits.B.RaghuKanthetal explains the advantages of using reversible logic gates in the implementation of circuits. It decreasesgarbage outputs, number of gates utilized. Author realized the addition and subtraction operations using DKGgate. The results are compared with circuits which are made with conventional gates. The newly proposedadder/subtractorcircuitcanbeappliedvastlyinthedesignofthenanotechnology[4]whichhaswideapplications.

T. Himanshu described that the reversible logic has emerged as a promising technology have applications inquantum computation. The gates such as AND, OR and EX-OR will not work as reversible gates. This work [3]is done by a newly proposed reversible gate called “SMG”. This gate is useful in manufacturing faster andpowerful adder circuits. Yedukondala Rao, explained the reversible TSG gate, Fredkin gate, Toffoli gate used todesign the four-bit carry select adder. Proposed design of Carry Select Adder that will compare the powerdissipation with the existing work. They presented the design of Carry Select adder using TSG module andFredkin module. The quantum cost of the circuit is clearly explained in [7]. Ripple carry adder is one of theefficientadderswhichiseasytodesignandalsoeasytoanalysebutslowinprocessing.Inordertoachieve muchmore speed using carry look a-head adder is advisable but major drawback of this is consumes more area [6]. Bykeeping these two major drawbacks, carry select adder is advisable. In carry save adder is designed with HNGandPeresgate.TheHNGisusedinplaceoffulladderandPeresgateisusedonbehalfofhalfadder.These stagesare arranged in a binary tree structure to generate a sum and carry [9]. Ashima Malhotra, designed reversiblemultiplexerswhichhaslessquantumcostandlessareawhencomparedwithconventionalone.Iti sconstructed withthehelpofoperationintheFredkingate.Latertheoperationintheredkingateismodifiedwillevendecreasesthe complexity incircuit design [5].

3.PROPOSED WORK

The first semiconductor chips held one transistor each. Subsequent advances added more and moretransistors, and, as a consequence, more individual functions or systems were integrated over time. The firstintegrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors,making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far pastthis mark

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and today's microprocessors have many millions of gates and hundreds of millions of individualtransistors.

At one time, there was an effort to name and calibrate various levels of large-scale integrationabove VLSI. Terms like Ultra-large-scale Integration (ULSI) were used. But the huge number of gates andtransistorsavailableoncommondeviceshasrenderedsuchfinedistinctionsmoot.Termssuggestinggreaterthan VLSI levels of integration are no longer in widespread use. Even VLSI is now somewhat quaint, given thecommonassumption that all microprocessorsare VLSIor better.

Asofearly2008,billion-transistorprocessorsarecommerciallyavailable,anexampleofwhichisIntel's Montecito Itanium chip. This is expected to become more commonplace as semiconductor fabricationmoves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing newchallenges such as increased variation across process corners). Another notable example is NVIDIA's 280 seriesGPU.

This microprocessor is unique in the fact that its 1.4 Billion transistor count, capable of a teraflopof performance, is almost entirely dedicated to logic (Itanium's transistor count is largely due to the 24MB L3cache). Current designs, as opposed to the earliest devices, use extensive design automation and automated logicsynthesistolayoutthetransistors,enablinghigherlevelsofcomplexityintheresultinglogicfunctionality.Certainhigh-performance logic blocks like the SRAM cell, however, are still designed by hand to ensure the highestefficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance bytradingstability).

2.1*Whatis VLSI?*

VLSIstandsfor"VeryLargeScaleIntegration".This is thefield which

VLSI

1. SimplywesayIntegrated circuitismanytransistorsononechip.
2. Design/manufacturingofextremelysmall,complexcircuitryusingmodifiedsemiconductormaterial
3. Integratedcircuit(IC)maycontainmillionsoftransistors,eachafewmminsize
4. Applicationswideranging:mostelectroniclogicdevices

2.2*HistoryofScaleIntegration*

- late40sTransistorinventedatBellLabs
- late50sFirstIC(JK-FFbyJackKilbyatTI)
- early60sSmallScale Integration(SSI)
  - 10sof transistors on achip
- late60sMediumScale Integration(MSI)
  - 100sof transistors on achip
- early70sLargeScale Integration(LSI)
  - 1000sof transistor on achip
- early80s VLSI10,000sof transistors on a
  - chip(later 100,000s &now 1,000,000s)
- UltraLSIis sometimesused for1,000,000s
  - ✓ SSI-Small-Scale Integration(0-102)
  - ✓ MSI-Medium-Scale Integration(102-103)

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- ✓ LSI-Large-Scale Integration(103-105)
- ✓ VLSI-VeryLarge-Scale Integration(105-107)
- ✓ ULSI-UltraLarge-Scale Integration(>=107)

improve system characteristics in several critical ways. ICs have three key advantages over digital circuits builtfromdiscretecomponents:

- ✓ Size. Integrated circuits are much smaller-both transistors and wires are shrunk to micrometresizes, compared to the millimetre or centimetre scales of discrete components. Small size leads toadvantages in speed and power consumption, since smaller components have smaller parasiticresistances,capacitances,and inductances.
- ✓ Speed. Signals can be switched between logic 0 and logic 1 much quicker within a chip than theycanbetweenchips.Communicationwithinachipcanoccurhundredsoftimesfasterthancommunicationbetweenchipsonaprintedcircuitboard. Thehighspeedofcircuitson-chipisduetotheirsmallsize-smallercomponentsandwireshavesmallerparasiticcapacitancestoslowdownthe signal.
- ✓ Powerconsumption.Logicoperationswithinachipalsotakemuchlesspower.Onceagain,lowerpower consumption is largely due to the small size of circuits on the chip-smaller parasiticcapacitancesand resistances requireless power to drivethem.

2.3 *VLSIandsystems*

Theseadvantagesofintegratedcircuitstranslateintoadvantagesatthesystemlevel:

- ✓ Smallerphysicalsize.Smallness isoftenanadvantageinitself-considerportabletelevisionsorhandheldcellulartelephones.
- ✓ Lower power consumption. Replacing a handful of standard parts with a single chip reducestotal power consumption. Reducing power consumption has a ripple effect on the rest of thesystem:asmaller,cheaperpowersupplycanbeused;sinceless powerconsumptionmeanslessheat,afanmaynolongerbenecessary;asimplercabinetwithlessshieldingforelectromagneticshielding may befeasible, too.
- ✓ Reduced cost. Reducing the number of components, the power supply requirements, cabinetcosts,andsoon,willinevitablyreducesystemcost.Therippleeffectofintegrationissuchthatthe cost of a system built from custom ICs can be less, even though the individual ICs costmorethan thestandard parts they replace.

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Understanding why integrated circuit technology has such profound influence on the design of digital systemsrequiresunderstandingboththetechnologyof ICmanufacturingandtheeconomicsof ICsanddigitalsystems.

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Electronic systems now perform a wide variety of tasks in daily life. Electronic systems in somecases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics areusually smaller, more flexible, and easier to service. In other cases electronic systems have created totally newapplications.Electronicsystemsperform a varietyof tasks, someofthemvisible, somemorehidden:

- ✓ Personal entertainment systems such as portable MP3 players and DVD players performsophisticatedalgorithms with remarkably littleenergy.
- ✓ Electronicsystemsincarsoperatestereosystems anddisplays;theyalsocontrolfuelinjectionsystems, adjust suspensions to varying terrain, and perform the control functions required foranti-lockbraking (ABS)systems.
- ✓ Digital electronics compress and decompress video, even at high-definition data rates, on-the-fly inconsumer electronic
- ✓ Low-cost terminals for Web browsing still require sophisticated electronics, despite theirdedicatedfunction.
- ✓ Personal computers and workstations provide word-processing, financial analysis, and games.Computersincludebothcentralprocessingunits(CPUs)anddspecial-purposehardwarefordiskaccess, fasterscreen display,*etc*.
- ✓ Medicalelectronicsystemsmeasurebodilyfunctionsandperformcomplexprocessingalgorithms to warn about unusual conditions. The availability of these complex systems, farfromoverwhelming consumers,only createsdemand foreven morecomplex systems.

Thegrowingsophisticationofapplicationscontinuallypushesthedesignandmanufacturingofintegratedcircuitsandelectronicsystems to new levels ofcomplexity.

And perhaps the most amazing characteristic of this collection of systems is its variety-as systems become morecomplex,webuildnotafewgeneral-purposecomputersbutanever widerrangeofspecial-purposesystems.Ourabilitytodosoisatestamenttoourgrowingmasteryofbothintegratedcircuitmanufacturinganddesign,buttheincreasingdemands of customers continueto test thelimits ofdesign and manufacturing

4.SIMULATION RESULT

The Efficient Ladner-Fischer adder is designed on VHDL (very high speed integration hardwaredescriptionlanguage).Xilinxprojectnavigator12.1isusedforsynthesis.Simulationresultsareshownin Fig 4. The design of adders is done on VHDL. The memory and delay performance Efficient Ladner-Fischer adder(ELF) isshown inTable1. Table 1.Delayand memory usedin ELF.

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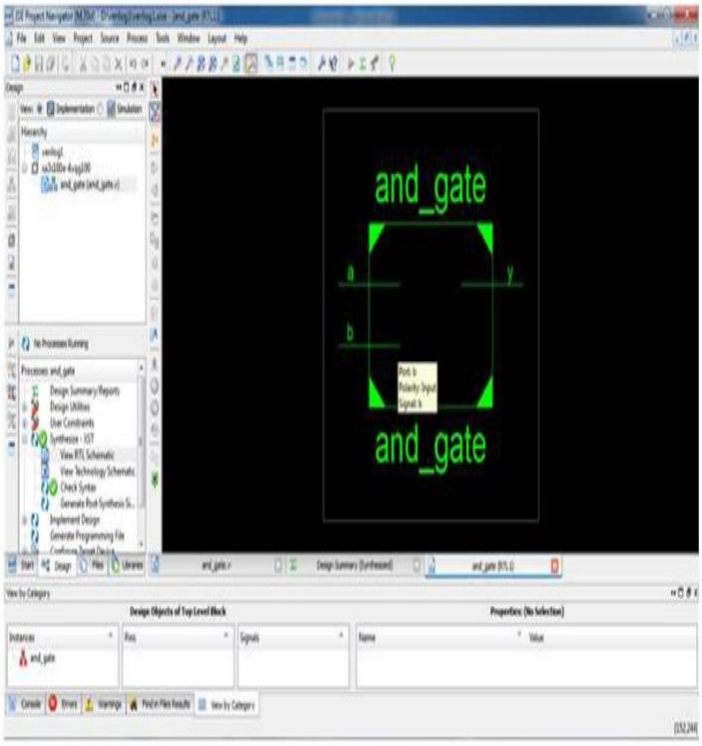

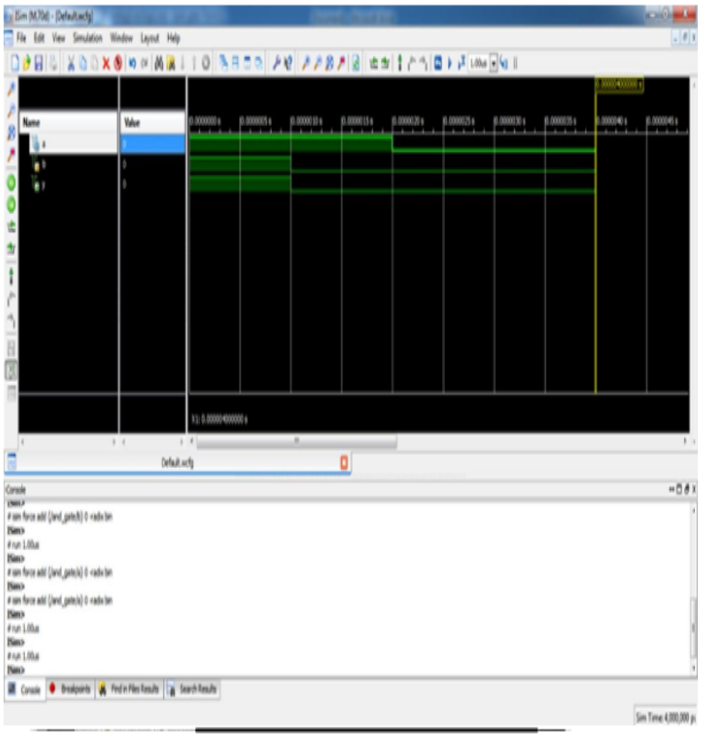

5.CONCLUSION

Inthisproject,anewapproachtodesignanEfficientLadner-FischerAdderconcentratesongatelevelstoimprove the speed and decreases the memory. It is like tree structure and cells in the Carry Generation Stage aredecreased to speed up the binary addition. The Proposed Adder addition operation offers great advantage inreducing delay. The future scope is to design 32 Bit Proposed Adder with less number of black cells to improvetheareaand delay performanceof the adders.

6.REFERENCES

[1] Pakkiraiahchakali,madhukumarpanel“Design OfhighspeedLadner-Fischerbasedcarryselectadder”IJSCEmarch2013

[2] Davidhikeshoe,ChrisMartinezandsrijyothsnavundavalli“Designandcharacterizationofparallelprefixaddersusing FPGAs“, Pages.168-172, march2011IEEE.

[3] K.VitoroulisandA.J.Al-Khalili,“performanceofparallelprefixaddersimplementedwithFPGAtechnology,” IEEENortheastWorkshoponcircuitsandsystems, pp.498-501, Aug.2007.

[4] Haridimost.vergos,Member,IEEEandGiorgos Dimitrakopoulos,Member,IEEE,”Onmodulo2n+1 adderdesign”IEEETrans on computers, vol.61, no.2, feb 2012

[5] GiorgosDimitrakopoulosandDimitrisNikolos, “High-SpeedParallel-PrefixVLSILingAdders”IEEETransoncomputers, vol.54, no.2, Feb. 2005.

[6] S.Knowles,"Afamily ofadders," Proc.15 th Symp. Comp. Arith.,pp.277-281,June2001[7]R.LadnerandH.Fischer,"Aregularlayoutforparalleladders",IEEETrans.Computers, vol.C-31,no.3,pp.260-264,March1982.

[8] R.E.LadnerandM.J.Fischer,"ParallelPrefixComputation,"J.ACM,vol.27,no.4,pages831-838,Oct.1980.