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DESIGN AND ANALYSIS OF LOW POWER HYBRID CMOS FULL ADDER

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Abstract: In this project, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. We also propose six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, powerdelay product (PDP), driving ability, and so on.An efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style is proposed in this project. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy fullswing and fairly balanced outputs.we can extend this project for designing of full adder design and it's topologies

INTRODUCTION

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Now a day's power is the primary concern due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption.

The motivations for reducing power consumption differ application to application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally For the high performance non battery operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability.

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend.

Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices and wireless communications systems which demand high-speed computation and complex functionality with low power consumption. In these applications, average power consumption is a critical design concern. From the environmental viewpoint, the smaller the power dissipation of electronic systems, the lower the heat pumped into the rooms, the lower the electricity consumed and hence the lower the impact on global environment.

1.1 Need for Energy efficient Adders

Adders are the most important components used in most of the Digital signal processors for real time applications. Adders are also used in the architecture of other arithmetic operators like Subtractors, Multipliers, shifters, MACs, etc. Many Adder architectures have been proposed by various researchers over the years. Even today the researches on Adder architectures are finding a major interest for achieving energy efficient devices. The survey on conventional adder architectures [3, 5-9] have proved there is a lot more scope for optimization. One method of optimization is by using different logic styles for

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different parts of the design instead of using the same logic style throughout the design. This method of designing with different logic styles in various parts of the same circuit is called Hybrid circuit. Various hybrid architectures were surveyed for reference [1, 2 and 4].

This paper presents a Hybrid full adder circuit consisting of two different logic styles namely CMOS logic and Pass transistor logic. This method has lesser power consumption, and hence energy efficient.

1.2 LITERATURE SURVEY

We see many distributed papers thatcompete in outlining better circuits. Such reviews for the most part relyon inventive outline thoughts yet don't take after an efficient approach.As a result, the vast majority of them experience the ill effects of some unique disservices.

1) They are executed with rationale styles that have an incompletevoltage swing in some interior hubs, which prompts staticpower dissipation.2) Most of them experience the ill effects of extreme yield flag debasement andcannot maintain low-voltage operation.3) They prevalently have dynamic power utilization fornon-adjusted spread deferral inside and outside circuits,which brings about glitches at the outputs.Therefore, an efficient outline procedure can be respected asa solid answer for the test. It is not attempt and-blunder driven,which implies that it efficiently and intentionally plans to the designgoals. It likewise picks circuit parts astutely and does not postponethe assurance of the circuit attributes after recreation. Celldesign approach (CDM) has been exhibited to plan some limitedfunctions, for example, two-input XOR/XNOR and carry–inverse carryin the half breed CMOS style. The transcendent outcomes persuadeus to enhance CDM through two phases: 1) producing more complexfunctions and 2) correcting some residual blemishes. The imperfections inpreviously distributed CDM incorporate containing some manual strides inthe configuration stream and producing an extensive number of outlines in whichthe transcendent ones would be resolved after the consummation ofsimulations. In this way, in the principal arrange, a three-input XOR/XNORas a standout amongst the most intricate and universally handy three-input fundamental gatesin number juggling circuits has been picked. In the event that the productivity ofthe circuits is affirmed in such a focused domain, it canshow the quality of the approach. In the second stage, CDM ismatured as methodical CDM (SCDM) in outlining the three-inputXOR/XNORs interestingly. It methodicallly produces elementarybasic cell (EBC) utilizing parallel choice graph (BDD), and wiselychooses circuit parts in view of a particular target. This takesplace when the specified elements are not considered in the CDM.Therefore, after the efficient era, the SCDM considerscircuit streamlining in light of our objective in three stages: 1) savvy selectionof the fundamental cell; 2) astute determination of the alter mechanisms;and 3) transistor measuring. It ought to be noticed that BDD can be utilizedfor EBC era of other three-input capacities. We consider thepower-defer item (PDP) as the outline target. It remains as a fairperformance metric, definitely including convenient electronic systemtargets. The inspiration to utilize this procedure is the nearness ofsome remarkable components and the capacity to deliver some effective circuitsthat appreciate every one of these favorable circumstances.

1) The SCDM isolates a circuit structure into a principle structureand improvement redress systems. In the fundamental structure,it considers highlights including minimal number of transistorsin basic way, genuinely adjusted yields, being force sans ground, and symmetry. The components have the dutyof finishing the usefulness of the circuits, maintaining a strategic distance from anydegradation on the yield voltage, and expanding the drivingcapability.

2) minimal number of transistors in basic way builds thechances of the circuit to have better qualities, as experimentalresults have demonstrated a normal sparing of 10%–50% and27%–77% as far as deferral and Energy-Delay Product (EDP),respectively.

3) The dynamic utilization enhancement originates from the reality ofwell-adjusted spread postponement. This element is advantageousfor applications in which the skew between arriving signals iscritical for appropriate operation, and for fell applications toreduce the shot of making glitches.

4) Power sans ground primary structure prompts control lessening.

5) Symmetrical structure, high measured quality, and normal arrangementof outlines offer ascent to sharing more wells ofconnected transistors and thusly diminishing the possessed areaabout 26%–32%.

6) The corruption in all yield voltage swing can in this way becompletely evacuated, which makes the outline manageable inlow VDD operations and low static power dispersal.

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7) Internal rationale structure of plans can possibly be vitality efficientabout 17%–53% because of the joined decrease ofpower utilization and engendering delay.
8) SCDM uses the advantages of various rationale styles as the hybridstyle.
9) The technique has high adaptability in target and systematicallyconsider it in the three outline steps. This can lead toefficient circuits as far as execution, power, PDP, EDP,area, or a blend of them.
10) The quick advancement of microelectronics manufacture processesdemands another cell library era or a library technologymigration. The efficient deliberate strategy leadsto mechanized stream, which can lessen configuration time and costs,provide consistency in the cell library era process,increase the scope of recreation abilities at the characteristicsstep, and also limit the danger of mistakes.

EXISTING SYSTEM

The state-of-the art issues in this brief can be divided into twocategories as they are extracted from the topic: 1) conventional three inputXOR and 2) methodologies. Most of the designed SUMs havebeen produced jointly or by cascading some modules. The cascadedmodules derived from reformulations of the Boolean function, such as

$SUM = C_{in} \oplus H$ (1)

$SUM = C_{in} \cdot H\_ + C_{in} \cdot H$ (2)

$SUM = C_{in} \cdot H\_ + C_{out} \cdot H$, $C_{out} = C_{in} \cdot H + A \cdot H\_$ (3)

WhereH and Hare A⊕ B and the supplement of H, respectively.In (1), the H yield is XORed with convey of the previousstage (Cin). The SUM modules having a place with this class havebeen used in numerous adders, for example, SERF, XOR-FA, 9A, and 9Bas SUM module. Expression (2) can be realizedwith a two-to-one multiplexer with H and H_ as the selectlines, which is broadly utilized as a part of viper execution. In (3),carry from the past and this stage, Cin and Cout other than H and H_are utilized to create SUM yield. LPHS-FAis made up ofthe expression as a SUM module. At last, as specified some time recently, somecircuits mutually delivered the module from which we can point tothree-XOR, new-three-XOR, SUM-connect, SUM-PTL, 10T_new,12T_new, and 18T_new_FS. Among the majority of the mentionedcircuits, we consider the SUM modules of Hernandez1, Hernandez2,TFA, Hybrid, NEWHPSC, LPHS-FA, and 18T_NEW_FS, whoseexcellent execution are affirmed. As aresult, the total correlation will happen by choosing them forreference. As can be seen from the regular circuits, allthe distributed effective plans depend on inventive thoughts of designersThey don't take after an efficient approach, while new solutionsoften have enhanced couple of attributes, thus there is a free spacefor the orderly outline system. CDM has been used todesign some constrained capacities. In this concise, CDM is maturedas SCDM for planning three-input XOR/XNOR.

Full adders, being one of the most fundamental building blocks of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement1-bit full adder cells. The designs,
reported so far, may be broadly classified into two categories: 1) static style 2) dynamic style. In the existing system, full-adder has to obtain an intermediate signal and its complement, which are then used to drive other blocks to generate the final outputs. The overall propagation delay and the power consumption of the full-adder depend on the delay and its complement generated. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path**.**

In most hybrid techniques, XOR, and XNOR functions were simultaneously generated by pass transistor logic module by using only six transistors. CMOS module produces full swing outputs of the full adder but at the cost of increased transistor count and decreased speed. Although the hybrid logic styles offers promising performance, most of these hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included.

PROPOSED SYSTEM

Proposed XOR–XNOR Circuit

The nonfull-swing XOR/XNOR circuit of Fig. 1(a) [24] is efficient in terms of the power and delay. Furthermore, this structure has an output voltage drop problem for only one input logical value. To solve this problem and provide an optimum structure for the XOR/XNOR gate, we propose the circuit shown in Fig. 1(b). For all possible input combinations, the output of this structure is full swing. The proposed

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XOR/XNOR gate does not have NOT gates on the critical path of the circuit. Thus, it will have the lower delay and good driving capability in comparison with the structures of Fig. 1(a) and (b). Although the proposed XOR/XNOR gate has one more transistor than the structure of Fig. 1(b), it demonstrates lower power dissipation and higher speed. The input *A* and *B* capacitances of the XOR circuit shown in Fig. 2(b) are not symmetric, because one of these two should be connected to the input of NOT gates and another should be connected to the diffusion of nMOS transistor. Furthermore, the input capacitances of transistors *N*2 and *N*3 are not equal in the optimal situation (minimum PDP). Also, the order of input connections to transistors *N*2 and *N*3 will not affect the function of the circuit. Thus, it is better to connect the input *A*, which is also connected to the NOT gates, to the transistor with smaller input capacitance. By doing this, the input capacitances are more symmetrical, and thus, the delay and power consumption of the circuit willbe reduced. To clarify which transistor (*N*2 or *N*3) has largerinput capacitance, let us consider the condition that the inputschange from *AB* = 00 to *AB* = 10.

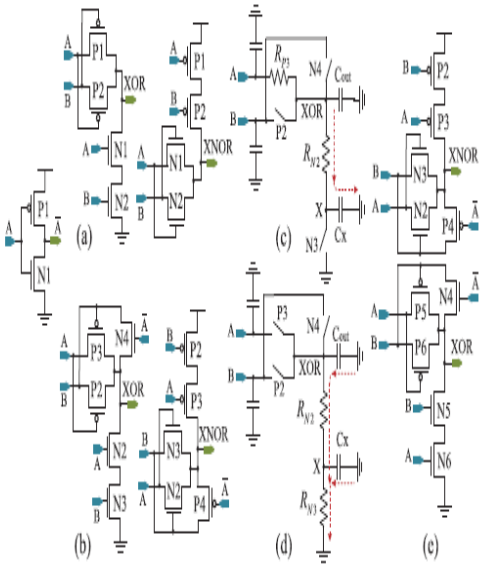

Fig. 2(e) shows the proposed structure of the simultaneousXOR–XNOR gate consisting of 12 transistors. This structureis obtained by combining the two proposed XOR and XNORcircuits of Fig. 2(b). If the inputs of this circuit are connectedas mentioned in Section III-A, the input *A* and *B* capacitancesare not equal (the inputs *A* and *B* are connected to the sametransistor count). Thus, to equal the input of capacitances, they are connected to the circuit, as shown in Fig. 2(e). In this case,the input capacitances are approximately equal and the powerand delay are optimized. This structure does not have any NOTgates on the critical path and its output capacitance is verysmall. For this reason, it is very high speed and consumeslow power. The delay of XOR and XNOR outputs of thiscircuit is almost identical, which reduces the glitch in thenext stage. Other advantages of this circuit are good drivingcapability, full-swing output, as well as robustness againsttransistor sizing and supply voltage scaling.We proposed six new FA circuits for various applicationswhich have been shown in Fig. 6. These new FAshave been employed swith hybrid logic style, and all of themare designed by using the proposed XOR/XNOR or XOR–XNORcircuit. The well-known four-transistor 2-1-MUX structure[Fig. 8(a)] is used to implement the proposed hybrid FA cells.This 2-1-MUX is created with TG logic style that has no staticand short-circuit power dissipation.

Fig. 6(a) shows the circuit of first proposed hybrid FA(HFA-20T) which is made by two 2-to-1 MUX gates and the XOR–XNOR gate of Fig. 2(e). The circuit of HFA-20T has not high power consumption NOT gates on critical path and consists of 20 transistors. The advantages of this structure are full-swing output, low power dissipation and very high speed, robustness against supply voltage scaling, and transistor sizing. If *A* _ *B* = 1, then the output *C*out signal equals to the input signal *A* or *B*. But to equalize the inputs capacitance, both of the input signals *A* and *B* are used for implementation and are connected to the transistors *N*9 and *P*10 [in Fig. 6(a)], respectively. The only problem of HFA-20T is reduction of the output driving capability when it is used in the chain structure applications, such as ripple carry adder. Of course, this problem exists in the circuits that use the transmission function theory in their implementation without buffering output. Fig. 7 shows the circuit layout of proposed HFA-20T which designed for minimum power consumption [26]. One way to reduce the power consumption of the FA structures is to use a XOR/XNOR gate and a NOT gates to generate the other XOR or XNOR signal. The proposed hybrid FA cell (HFA-17T) shown in Fig. 6(b) is designed by using the XOR gate of Fig. 2(b).

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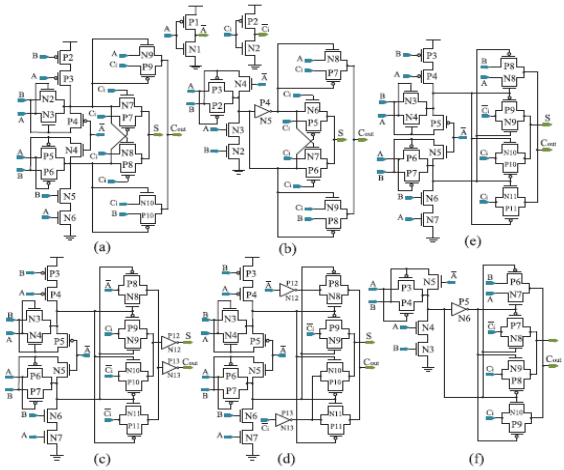
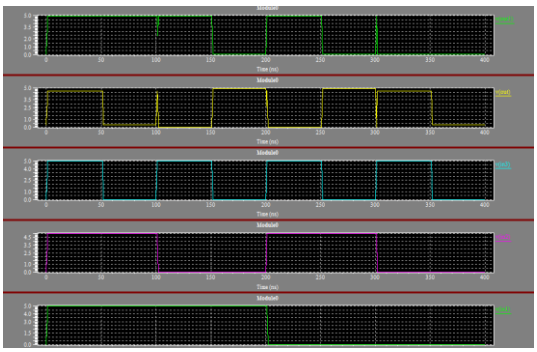


Fig. 6. Proposed six new hybrid FA circuits. (a) HFA-20T. (b) HFA-17T.(c) HFA-B-26T. (d) HFA-NB-26T. (e) HFA-22T. (f) HFA-19T.

This structure is made by 17 transistorsthat has three transistors less than the HFA-20T. The delay ofHFA-17T is higher than that of HFA-20T due to the addition
of NOT gates on the critical path of the HFA-17T (for making
the XNOR signal from the XOR signal). It may be expectedthat the power consumption of HFA-17T is less than that ofHFA-20T due to the reduction in the number of transistors. Butthe NOT gate on the critical path of the circuit increases theshort circuit power. So there is no significant reduction in totalpower dissipation of the HFA-17T. Also, the NOT gate willslightly improve the output driving capability of the circuit.As mentioned earlier, using the buffer on the output of acircuit is almost mandatory, especially in applications thatthe output capacitance of each stage is high. In practice,
the driving capability of VLSI circuits is degraded due to thecreation of the parasitic capacitors and resistors during thefabrication, as well as increasing the threshold voltage oftransistors over the time, but the output buffer improves thissituation. Fig. 6(c) presents the third proposed hybrid FAwith buffers on the *Sum* and *C*out outputs (HFA-B-26T),and it is made with 26 transistors. There are XOR–XNORgate, one 2-1-MUX gate, and NOT gates on the critical pathof HFA-B-26T. The output NOT gates are used to prevent thedriving output nodes by the inputs of the circuit and alsoreduce the resistance from the output node of the circuit tothe sources (*V*DD and GND). The power consumption anddelay of HFA-B-26T are more than that of HFA-20T andHFA-17T FAs. Fig. 6(d) shows another proposed hybrid FAwith new buffers (HFA-NB-26T), where they are placed in thedata inputs of 2-1-MUX gates instead of placing the buffers inthe outputs. If the input signals of *A* and *C* are produced by thebuffer, then for all possible input combinations, the *Sum* and*C*out outputs are not driven by the inputs of the circuit. To dothis work, three additional NOT gates are enough, becausethere was already the *A* signal and can be made the buffered *A*signal with an extra NOT gate. So the HFA-NB-26T FA circuitis made by 26 transistors. The data input nodes of 2-1-MUXsreach to their final value (GND or *V*DD) before the XORand XNOR signals are produced. Thus, the critical path ofHFA-NB-26T consists of an XOR–XNOR gate and a 2-1-MUXThe driving capability of the HFA-NB-26T is slightly less thanthat of HFA-B-26T due to existing the 2-1-MUX gate betweenthe buffer and the output node [which increases the resistancefrom the output node to the sources (*V*DD and GND)].The circuits of HFA-20T and HFA-17T have been designedso that the less number of transistors has been used. To producethe output *Sum* signal, the XOR, XNOR, and *C* signals are onlyused so no additional NOT gates needs to generate the *C* signal,whereas if the *C* signal is also used to produce the *Sum* output,then XOR and XNOR signals will not drive the *Sum* outputthrough the TG multiplexer, but only they will be connectedto the data select lines of 2-1-MUX. So the capacitance of XORand XNOR nodes become smaller, and the delay of the circuitwill be improved. It is expected that the power consumption and delay ofthe HFA-22T and HFA-19T FA circuits are less than that ofHFA-20T and HFA-17T, respectively (despite having two moretransistors), due to the less capacitance of XOR and XNORnodes. Also, by adding the *C* signal, the driving capability ofHFA-22T and HFA-19T will be better than that of HFA-20Tand HFA-17T, respectively.

SIMULATION RESULT



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COMPARISION TABLE

EXISTING METHOD	PROPOSED METHOD	
TRANSISTOR COUNT	26	22
Control CONSUMED	3.96 mW	1.392 mW
DELAY	1.40 sec	0.89 sec
Most extreme POWER CONSUMED	5.529882e-005	2.598204e-005
Least POWER CONSUMED	3.926799e-009	1.392061e-009
Normal POWER CONSUMED	8.678680e-007	1.451884e-007
TRANSIENT ANALYSIS	0.03 sec	0.01 sec

CONCLUSION AND FUTURE SCOPE

SCDM fills in as a plan technique for three-input XOR/XNOR, which is a standout amongst the most perplexing and focused and also generally useful three-input fundamental entryways in math circuits. The philosophy puts accentuation on doing every one of the means in a totally deliberate manner. It likewise appreciates high flexibility in configuration target, while it takes after a similar methodology to acquire the cutting edge plans. This brief has favored SCDM with the shrewd choice of the circuit parts for the PDP target. At last, three new superior three-input XOR/XNOR circuits with less PDP and involved zone are imagined utilizing SCDM. The new circuits appreciate higher driving capacity, transistor thickness, commotion insusceptibility with low-voltage operation, and minimal likelihood to deliver glitches. As a one of a kind element, the basic way of the exhibited outlines comprises of just two transistors, which causes low spread postponement. All things considered, these circuits outflank their partners with 17%–53% and 27%–77% change in PDP and EDP, separately, in HSPICE reenactment in light of the TSMC 0.13-µm innovation. The range use for the proposed circuits appreciates 26%–32% change with the upsides of consistency and symmetry in format.

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