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An Efficient Frequency Multiplier with DLL-Based Clock Generator for SoC Applications

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Abstract: Any implementation of something like a specific form of the multiplier in automated frequency measurement systems depends primarily on the overall permitted variance of both the output frequency of that same transducer. Therefore, it will be usually best to always use frequency multipliers of that first category in transducers with such a slight variance. The suggested edge incorporates optimal speed and reliable activity that used an organizational structure as well as an unselected overlap. The suggested hybrid digital edge solution provides broadband with low-energy and low-area benefits as well as being a potential candidate for low-energy frequency summaries in deep CMOS sub-micrometer. A charge pump was substituted by a counter to integrate the automated interface. The overall system consists of all the resources for doing the operation of stable clock pulses for SoC applications as well as the frequency multiplier. In this paper, the frequency multiplying method is carried out how to use a clock amplification system based on an edge combiner, which is carried out using the C2MOS logic.

Index Terms: Low power, frequency multiplier, phase detector, clock

I. INTRODUCTION

The systems of low power and low-area (TX) transmitters are important regarding short-range communications e.g. wireless transmission networks, body area networks, and certain other battery-operated applications. Such low-power systems have relaxed vibration, spectral purity, and architecture criteria. Phase-locked TXs (PLL) are indeed effective and area-efficient compared to the traditional mixer-based TX direct update design. The energy demand in a frequency synthesis can indeed be reduced by operating the PLL in lower frequencies and by using frequency multiplier circuits without the loop to build the modified RF carrier .The power requirements in a frequency synthesis can be decreased by operating the PLL in lower frequencies.

The strategy of low power architecture is often used to reduce SoC power usage. The power demand is categorized into static or dynamic. Few low power architecture approaches including Dual Voltage Supply (dual V_{dd}) and Dual Threshold (dual V_{th}) Single Threshold CMOS (MTCMOS) are being used to minimize static power usage. To minimize dynamic power requirements, a low power modeling approach termed Dynamic Voltage Scaling and Dynamic Frequency Scaling has been used by regulating the voltage and frequency at workload to minimize dynamic power requirements. Frequency clock generation with a frequency multiplier is needed for scaling by using PLL (Phase Locked Loop) or DLL (Delay Locked Loop). DLL is safer than PLL because of higher cost cycles and latency aggregation in PLL. The DLL-based clock generator for the multiplier is therefore used and comprised of a pulse generator, a power logic, and even an edge combiner. Therefore it is more suited for realistic use [1-2].

To address this issue, multiple DLL-based clock generators were introduced. The DLL clock generator consists of the DLL center and the frequency multiplier and is normally split into two blocks: Pulse Generator and Edge Combiner. If multiplication of variable frequencies is needed, a multiplication ratio control circuit is introduced. Multiphase clocks are

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produced employing an input clock in the DLL path. The pulse generator produces the number of pulses needed by the multiplication-ratio signal generator from multiple-phase clocks to combiner circuit produces a multiplied clock by using the pulses chosen. In addition, the N/2 number of multiphase clocks is the full operation for both the frequency multiplier. Because while the frequency generator gathers several clocks, jitter aggregation sometimes does not happen. However, the frequency multiplier can adjust multiplication ratios quickly. Furthermore, the conceptual range or performance load of the frequency multiplier should be expanded to raise the multiplication ratio [8-10]. Moreover, the average clock frequency is significantly diminished.

The main contributions and organization of this paper are summarized as follows: In section, 2 we describe background details of DLL based clock generators details. The section 3 proposed work. The section 4 deliberates results and discussions. Finally in section 5 we concluded the paper.

II. BACKGROUND WORKS

In [3], the author's paper envisages a high level of complications and a time-consuming workload for the development of multimedia applications. Many of the DVS algorithms, which are a productive and useful technique for classifying these DVS algorithms by outstanding multimedia applications, have been advocated for real-time use. In this paper, they advocate the new offline linear programming technique for regulating the low energy usage for multimedia processing tasks within delays. Due to the lower energy content accessed, they examined the greatness of DVS algorithms. Subsequently, they enhance the LP formulation to build an online DVS algorithm for multimedia real-time, based entirely on powerful sequential linear programming.

In [4] the authors study conventional stepping voltage system and involve a delay margin to ensure that all possible device and wiring process deviations and temperature inconsistency continue at a certain level of firmness. This margin is needed if the critical path is to be changed because of such improvements. Furthermore, because of the slower interconnection delay, a critical path changes from operating voltage to each other with voltage particularly in comparison to the logical delay. To ensure a faultless operation with a high limit, technological scaling challenges both process variation and interconnect delay. Such a margin is insufficiently converted into upward voltage and corresponding energy. In addition, voltage-scaling features of certain critical paths are followed by logical programming and delay lines interconnected to perform the same delay sequences as the actual critical path.

In [5], the authors present a delay-locked (DLL) clock generator with several unique advantages over the traditional phase-locked-loop generator, namely no jitter growth, fast locking, the balance of loop production and the easy combination of the loop filters. To overcome the conservative DLL-based system's constrained locking range and frequency multiplication problem, they suggest a reset circuitry phase detector and a new frequency multiplier. It is made in a CMOS process of 0.35µm. Our DLL clock initiator covers an area of 0.07 µm and is 42.9 mW power consumption. It has an operating range of 120 MHz-1, 1 GHz and a cycle to cycle jitter of 1 GHz is accurate. The Die area, peak to peak and R.M.S. jitter are the smallest possible three parameters of comparison. These parameters pertain to those of multipliers with high-frequency clocks.

In [6], the authors offer a frequency multiplier composed of a monolithic local CMOS oscillator in the DLL technique that organizes a low noise 900 MHz carrier frequency. This example supports the necessity of a dual-mode-137 AMPS / TDMA standard. In [7], the Author DLL-

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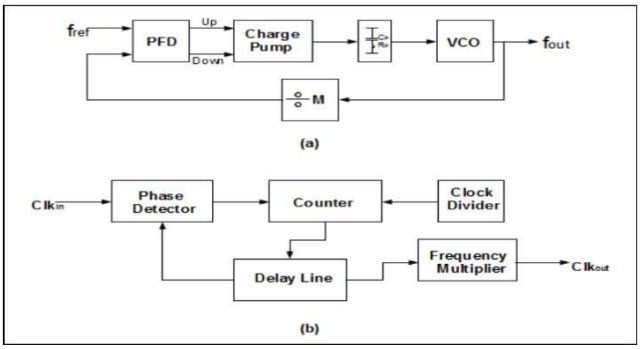
based frequency synthesizer. A delay-locked loop is designed for the Mode-1 UWB system. With the acceptable 528-MHz input frequency, this frequency synthesizer delivers less than 9.5-ns adjustment time. This frequency of reference uses broad bandwidth and rapid sales architecture. Besides, a

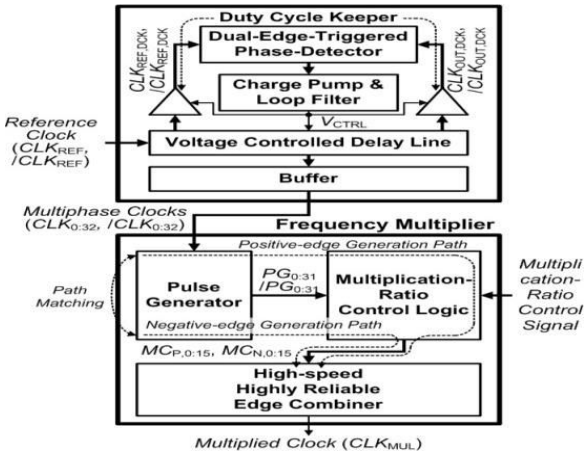


discreet time model and DLL's analytical model for phase noise are foreseen in this work. Research results demonstrate high availability with predicted adjustment time and phase noise.

III. PROPOSED MODEL

The block diagram for binary frequency-shift-keying (BFSK)/amplitude multiplication frequency changes with small area penalties. Because only another PD-N is applied for each edge combiner differential result while the cumulative multiplication rate is too high by one, the edge combiner's performance load rises slower than even for the combiner unit. The primary requirement of the multiplier is to get the required clock signals that are generated from the DLL clock generator and simultaneously D flip-flop gets the multiphase clocks. Because of control logic, the correct pulses are obtained with logic. All the phase clocks are delivered during the time of neighbor clocks that are delayed by the same period, which in return produces pulses from the clock signals. Eventually, whenever the multiphase clocks move through the multiplication rate control logic, device-timing distortion will arise, which in turn will produce pulses appropriate for high frequency, consumes less quantity of power and area with various clock speeds.

For signal synthesis, various methods can be employed, in which either an oscillator is worked directly at the target frequency or a sub-harmonic. Even though the activity of an oscillator at the target frequency might be the most power-efficient choice, relying on process technology it often provides a range



of disadvantages. The frequency of the transistor oscillation is restricted to that of the highest level, the phase noise as well as the tuning region based on the efficiency variable as well as the tuning range of the resonator. Besides, with all the multiplication factor the edge loading decreases quickly.

Figure 1: Overview of System clock operation

The diagram below displays two multipliers that can also during operation for performing multiplications with high speed. In fig.2 (a) The PLL arrangement indicates that the reference clock correlation. As illustrated in fig. 2(b) contains counter and clock divider with software constructs are presented.

Figure 2: Process of Frequency multiplication (a) Circuit relies on PLL (b) Circuit relies on DLL

In Fig.2, the reference clock frequency is linked to the reference clock for a bit-controlled delay line produced with the original delay sensitive signals for configurations. In comparison to either the non-ideal transition properties, the effects of the high-frequency approximation would be further varying from those in the previous ideal signals review, as the influence of

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parasite responsive components throughout the HBT decreases to reduce circuit output to higher frequencies. Further, in saturation regions, additional charges are added into the transistor foundation, impacting the clipping at high frequencies of the upper half-wave of the collector present. Since consistently the eight pulse is contrasted either with the reference clock and according to the phase difference, a new UP or DOWN signal is produced. This input process is followed for the period of locking time slot among variations in the unit when it is locked.

Sub-system with Frequency multiplier:

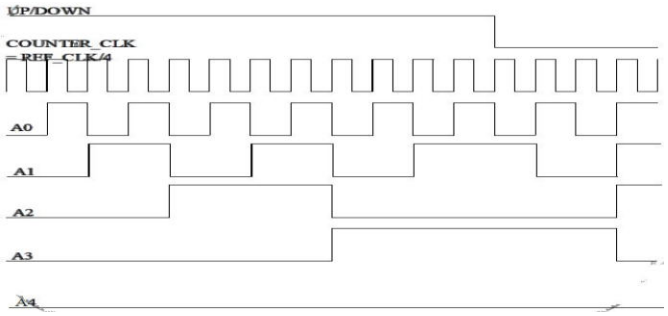
A. Clock Divider: This module produces clock pulses that are running at low speeds that is very much needed for subsystem working. By sub-system divisor unit is the input to which produces the frequency output clock equivalent to the operation of required clock/4. This comprises serially linked flip-flops of T type to reach the necessary clock frequency. The waveform of the clock divider is shown in Figure 3 below.

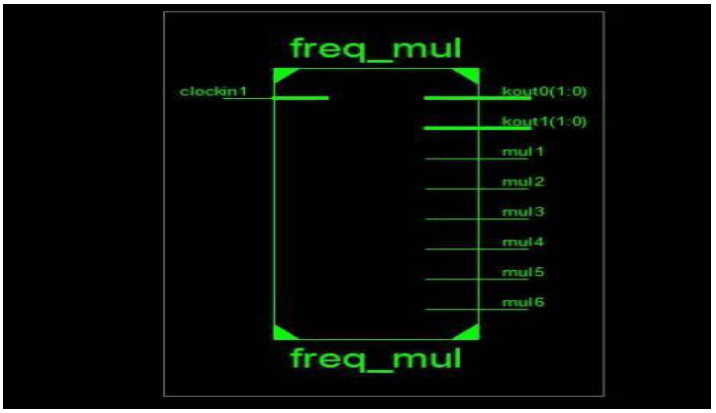
Figure 3: Clock waveform operation of divider unit

*B. **Phase Detector:*** The Phase Detector has been used to obtain a phase connection from either the delay line here between reference clock input as well as its delayed variant. To maintain a perfect synchronization relation for maintaining a consistent clock period without any delay for the model correspondingly. Figure 4 demonstrates the schematic diagram below. The phase detector circuit reflects the design of MS flip-flop.

Figure 4: Circuit associated with Phase Detector

*C. **Up-Down Counter:*** All other versions generate a certain output amount, as well as the respective amplitudes, which are identical. There seem to be optimum biasing levels from which the sixth harmonic amplitude is optimum, however, the 4th and 8th harmonic amplitudes are marginal and the evaluation of the signal has complied. Its operation mainly relies on the delayed pulse with one unit that is more reference to the phase detector unit generates several pulses makes it as a counter. As somewhat of a consequence, it reduces the delayed phase by rendering the delay section. Figure 5 below displays 5 counter waveforms, respectively.





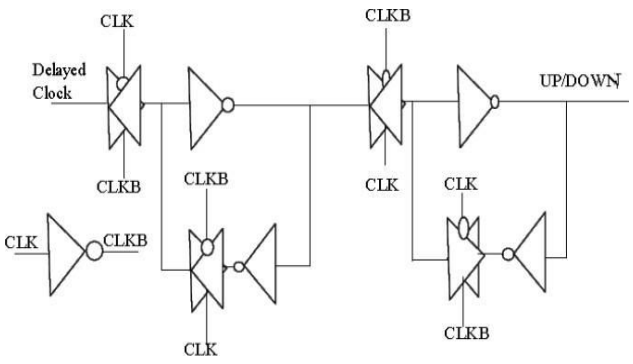


Figure 5: Up-Down Counter Waveform

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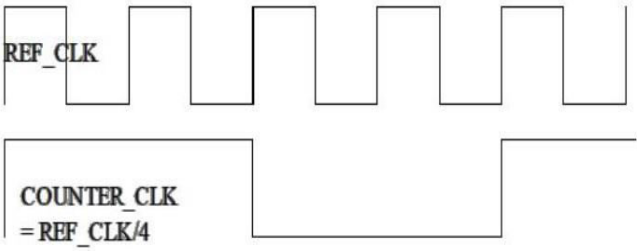

IV. RESULTS AND DISCUSSION

All the results are simulated with the help of Xillinx ISE design suite and coding is done with Verilog HDL.

Figure 6: RTL schematic

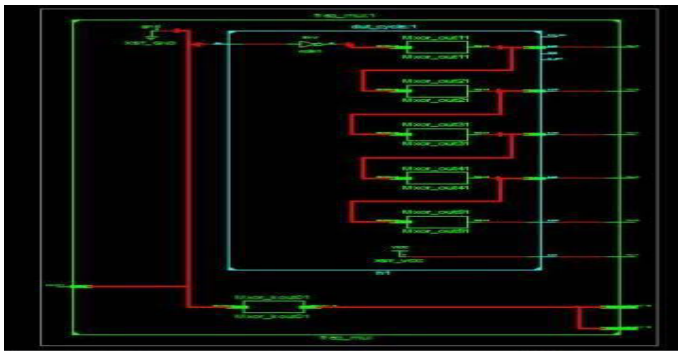

Figure 7: Technological view

Figure 8: Simulation output wave for DLL based frequency multiplier

Figure 9: Simulation output wave for Dual edge trigger counter

Figure 10: Simulation output wave for 32-different phase generator

V. CONCLUSION

In this paper, a frequency multiplier is recommended for a DLL clock generator. There seems to be no PLL component in this design rather than this counter and the clock divider is inserted into the framework. The optimized pulse generator, as well as the Multiplication Rate Control Logic, was suggested to increase the delay among positive and negative paths. Eventually, a computational review to verify the output is done. It is evident in contrast with other designs that this system absorbs less power than others do in the same phase.

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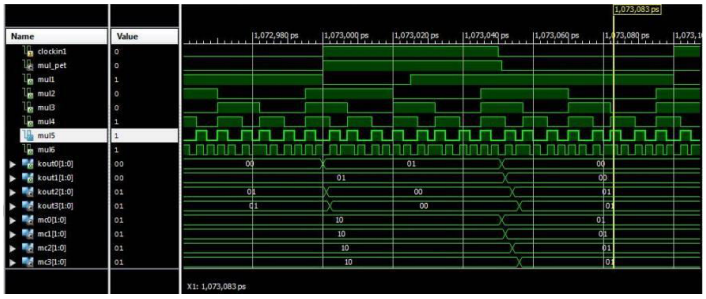

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