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DESIGN A LOW POWER FLIP-FLOP BASED ON A ADIABATIC TECHNIQUE

CHAVVA ANIL KUMAR REDDY[1], M.SUMA SREE[2]
[1]PG SCHOLAR.DEPT OF ECE, SIR C.V. RAMAN INSTITUTE OF TECHNOLOGY & SCIENCE, AP, INDIA
[2] ASST. PROFESSOR, DEPT OF ECE, SIR C.V. RAMAN INSTITUTE OF TECHNOLOGY & SCIENCE, AP, INDIA

Abstract:

In complementary metal oxide semiconductor circuit based designs, flip-flops are essential part of the clocking circuits. They are responsible for the synchronous-asynchronous behavior to the system. The basic circuit of flip flop that is used in various digital circuits determines the system power consumption. The type of flip flop used in digital circuits determines the output load of the circuits. In this paper we have presented adiabatic flip flops which are used for clocking in digital systems. The clocking scheme using energy recovery technique has already appeared as a successful and promising scheme for limiting power dissipation in ultra low power digital systems. Adiabatic flip flops are the key elements for this type of energy efficient adiabatic clocking scheme. The flip-flops are working in adiabatic principle. Here in this work we have done the simulation and analyze the performance of two basic types of energy recovery flip flops. These are single ended conditional capturing flip-flop and differential conditional capturing flip flop. Both the flip-flops are utilizing energy recovery scheme. For better comparison results we have also used clock gating scheme along with energy recovery technique.

1. INTRODUCTION

In complementary metal oxide semiconductor circuit based designs, flip-flops are essential part of the clocking circuits. They are responsible for the synchronous-asynchronous behavior to the system. The basic circuit of flip flop that is used in various digital circuits determines the system power consumption. The type of flip flop used in digital circuits determines the output load of the circuits. This is also known as clock load. This clock load directly affects the switching power consumption of circuits. Therefore, it is essential to introduce one technique to minimize the power consumption of flip flops to reduce the overall system power consumption. The power specification of modern portable digital circuits is severely limited. It is very essential to improve system power performance in the flip flop networks. Timing elements like flip-flops are very important for the performance of digital systems. This is due to the extremely large set up time and hold time. These are also essential for good performance and better efficiency. Recovery or recycling of energy in a circuit is a technique for low power digital circuits [5]. Energy recovery circuits can be designed to achieve low energy dissipations. This can be achieved by restricting the current to flow across circuit. As a result there is minimum amount of voltage drop across the circuit components. This type of circuits use pulsed power supply or sinusoidal power supply. In this scope, we have applied energy recovery or adiabatic techniques to the clock network. The basic signal which is used for clock supply is the most vital signal. Generally, the nature of the signal is capacitive. The principle used in energy recovery circuits is

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that, they recycle the energy from the output load capacitance to the input node. This happens during each operation cycle. The power consumption of the clock networks contributes more than 60% of the total power in high performance high speed VLSI systems [6]. Hence, low power clocking methodologies are essential for ultra low power design. Adiabatic flip-flops can use energy recovery process from the clock network. This results significant reduction of power dissipation. In single phase sinusoidal clock these low power flip-flops can operate. This clock can be generated with very high efficiency and energy recycling elements. We have implemented the clock based flip-flops in cadence digital simulator and obtained the results. In this project, we have discussed and compared two basic types of energy recovery flip flops. They are single ended conditional capturing energy recovery flip- flop (SCCER) and differential conditional capturing energy recovery flip flop (DCCER). We have estimated their power dissipation and timing specification constraints. We have also introduced clock gating technique. For the energy recovery clocked flip flops it is clearly seen that they reduce power consumption and propagation delay of the system.

2.LITERATURE SURVEY

Adiabatic dynamic logic

With adiabatic techniques for capacitor charging, theory suggests that it should be possible to build gates with arbitrarily small energy dissipation. In practice, the complexity of adiabatic approaches has made them impractical. We describe a new CMOS logic family-adiabatic dynamic logic (ADL)-that is the result of combining adiabatic theory with conventional CMOS dynamic logic. ADL gates are simple, general, readily cascadable, and may be fabricated in a standard CMOS process. A chain of 1000 ADL inverters has been constructed in 0.9 /spl mu/m CMOS and successfully tested at 250 MHz. This result, together with comprehensive circuit simulation, suggest that ADL offers an order of magnitude reduction in power consumption over conventional CMOS circuitry

A dual rail edge triggered latch

This paper describes a simple and compact dual-rail static edge-triggered latch (DSETL) with reduced latency over conventional static flip-flops. Power consumption of the DSETL is observed to be the lowest among high performance flip-flops. It consumes up to 51% less power than dual-rail hybrid latch-flip-flop and up to 25% less than conditional-capture flip-flop in practical circuits.

Flow-through latch and edge triggered flip-flop hybrid elements

This paper describes a hybrid latch-flipflop (HLFF) timing methodology aimed at a substantial reduction in latch latency and clock load. A common principle is employed to derive consistent latching structures for static logic, dynamic domino and self-resetting logi

H.Kawaguchi and T.Sakurai, A decreased clock-swing flip-tumble (RCSF) for 63% power reduction.

A diminished clock-swing flip-slump (RCSFF) is proposed, which is made out of a lessened swing clock driver and an uncommon flip-flounder which typifies the release momentum cutoff component. The RCSFF can decrease the clock framework energy of a VLSI down to 33% contrasted with the traditional flip-flounder. This power change is accomplished through the lessened clock swing down to 1 V. The zone and the postponement of the RCSFF can likewise be diminished by a factor of around 20%

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contrasted with the ordinary flipflop. The RCSFF can likewise diminish the RC postponement of a long RC interconnect to one-half.

Lessened clock-swing flip-flounder (RCSFF) is proposed to bring down the voltage swing of the clock framework. The schematic graphs of the ordinary flip-tumble and the proposed RCSFF. With the customary flip-slump, the clock swing can't be decreased on the grounds that and are required, and overhead ends up and coming if two clock lines and are to be circulated. Then again, if just is circulated, a large portion of the time related MOSFET's work at full swing, and just minor power change is normal. The RCSFF is made out of a genuine single-stage ace lock and a cross-coupled NAND slave-hook. The ace lock is a present hook compose sense-speaker. The striking component of the RCSFF is that it can acknowledge a lessened voltage swing because of the single-stage nature of the flip-slump. The voltage swing,Vclock , can be as low as 1 V.

V.Oklobdzija, V.Stojanovic, D.Markovic, and N.Nedovic,DigitalSystem ClockingHigh-Performanceand Low-Power Aspects .In CMOS multistage clock cradle plan, the obligation cycle of clock is at risk to be changed when the clock goes through a few cushion stages. The beat width might be changed because of unbalance of the p-and nMOS transistors in the long cradle. This paper depicts a deferral bolted circle with twofold edge synchronization for use in a clock arrangement process. Consequences of its SPICE reproduction, that identify with 1.2 lm CMOS innovation, demonstrated that the obligation cycle of the multistage yield heartbeats can be accurately changed in accordance with (50 ± 1)% inside the working recurrence run, from 55 MHz up to 166 MHz.

All contemporary computerized VLSI frameworks and other advanced frameworks depend on clock heartbeats to control the development of information. To achieve the most elevated circuit speed in CMOS applications, the clock dispersion framework must be painstakingly planned. A lot of consideration has been paid to clock recuperation, clock recovery, timing, and conveyance amid the most recent quite a long while.

B.Nikolic, V.G.Oklobdzija, V.Stojanovic, W. Jia, J.K.S.Chiu,and M. M.- T.Leung, Improved sense-enhancer based flip-flounder designand measurements.Design and exploratory assessment of another senseamplifier-based flip-tumble (SAFF) is displayed. It was discovered that the fundamental speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) hook in the yield organize. The new flip-tumble utilizes another yield arrange hook topology that fundamentally decreases delay and enhances driving capacity. The execution of this flip-flounder is checked by estimations on a test chip actualized in 0.18 m compelling channel length CMOS. Shown speed places it among the speediest flip-flops utilized as a part of the cutting edge processors. Estimation systems utilized in this work and in addition the estimation set-up are talked about.

V.Stojanovic and V.G.Oklobdzija Comparative examination of ace slave locks and flip-flops for elite and low-control frameworks .We propose an arrangement of principles for predictable estimation of the genuine execution and power highlights of the flip-flounder and master– slave hook structures. Another reenactment and enhancement approach is introduced, focusing on both high performance

3.EXISTING SYSTEM

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Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design 1, 2. Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In [9], a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13]. In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1" and "0" the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product(PDP) performances.

A. Conventional Explicit Type P-FF Designs

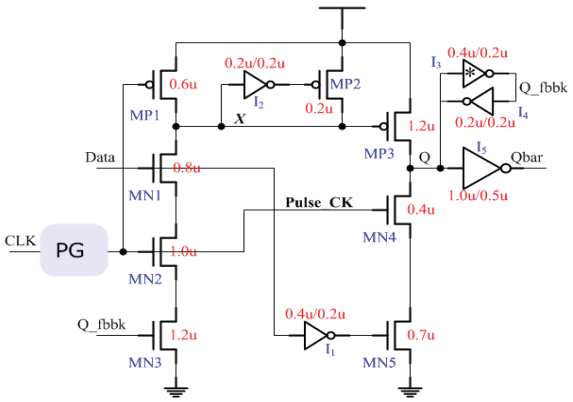

Fig. 1. Conventional P-FF designs. CDFF [16].

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are
generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its

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power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-closeto- output (ep-DCO) [7].

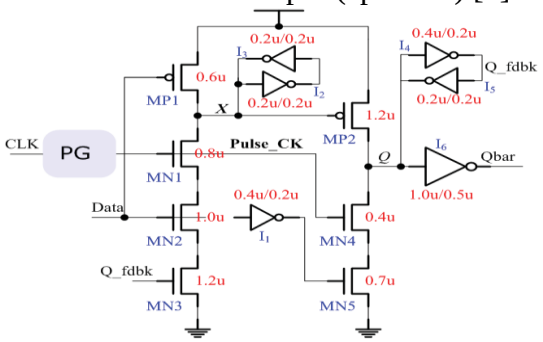

Fig. 2. Conventional P-FF designs Static-CDFF [17].

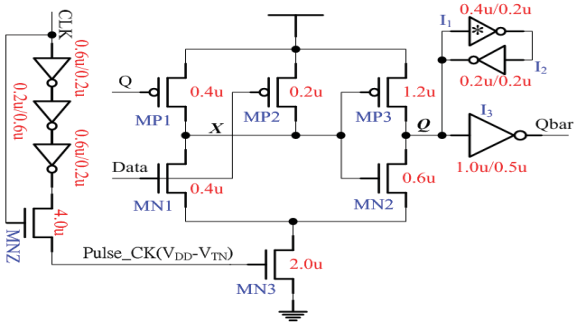

Fig. 3. Conventional P-FF designs. MHLFF [19].

It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed . An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input dataremains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only.

4.IMPLEMENTED SYSTEM ADIABATIC LOGIC

Conventional CMOS technology is very attractive and efficient method for low power circuit design. This is because of its minimum static power dissipation. Generally, conventional CMOS has two networks. One is PUN and another is PDN. Switching or dynamic power dissipation of CMOS circuits originates as a result of charging and discharging of load capacitance. This has a relationship with supply power clock and is proportional to the square of the power supply voltage of the circuit and frequency of switching clock. The circuit capacitance and frequency factors increase the power consumption of system. Therefore conventional CMOS design needs to be changed in order to satisfy the demand of low power supply. In Fig. 5.1 we have shown the equivalent circuit of charging adiabatic system. In adiabatic technique, output load capacitance is

charged by a constant current source. In conventional CMOS structures this is done by constant voltage source. The on resistance of PUN of PMOS network is represented by resistance, R and Co is the output capacitance [6].Constant current source resembles a voltage ramp. Now, the

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energy that is dissipated through adiabatic logic is given as

E(diss)= (Co Vdd/T)2.RT=RCo/T.CoVdd2----------(1)

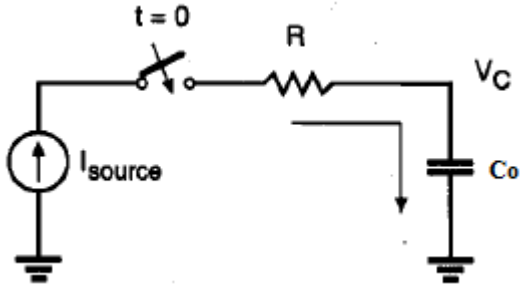

Figure 4. Equivalent circuit of adiabatic logic based circuits

It can be noticed that the energy dissipation is directly proportional to resistance R. Therefore, the energy dissipation can be limited by decreasing the on resistance through PMOS network. By using a current source which is constant throughout a switching event, the energy can be easily transferred from power supply to load capacitor. This can be done without any energy dissipation. Again, the energy stored in the load capacitance after charging process can be sent back to the power supply voltage. This is done by simply reversing the direction of current source [7]. The recycling of energy is a very attractive feature in adiabatic logic circuits. For this process, it is also called energy recycling logic. The constant current supply must be designed in such a way so that it can be capable of retrieving the charge back to the power supply. Adiabatic circuits use a special type of power supply which is constant. This source has a special feature. Instead of using the standard one, it uses pulsed power supply. There are many important design specifications which should be taken into account in any CMOS based adiabatic circuit design. The designers follow two basic design criteria. Firstly, the implementation should result in a power efficient design using the combination of power supply and clock generator. Secondly, a transistor operating in adiabatic mode must maintain some rules. The transistor must be always in on state when there is a significant current flowing through the transistors. The transistor must be off state when there is a significant difference between the source and drain voltages of the transistor [7].

5.3 PROPOSED DESIGN

SCCER FLIP-FLOP

Flip flops are the examples of sequential digital circuits. Generally in digital circuits four phase transmission gate (FPTG) flip-flops are used. They are very similar to the transmission gate based flip-flops that are used conventionally. Here we have presented two new adiabatic flip-flops which are more power and area efficient. These flip-flops can recover energy from their clock input capacitance which is the basic adiabatic principle.. That means, they have an energy recovery behavior. Their storage elements and internal nodes are powered by constant power supply. The SCCER flip-flop is nothing but single ended version of the DCCER flip-flop. The main circuit of SCCER flip-flop is shown in fig 2.There is pull up and pull down networks like MOS inviters. Pull up network contains one PMOS transistor MP1 and pull down network contains four NMOS transistors.MN1, MN2, MN3, MN4.The output QB controls the transistor MN3. It provides the conditional capturing. There is a static evaluation path in the right hand side. No conditional capturing process is required here.. Transistor MN3 is placed above MN4 in the stack. This placing of transistor reduces the sharing of charge in the circuit. That is achieved because, during the charge sharing event, the capacitance associated with transistor MN3 has already

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been charged. Therefore does not contribute to the charge sharing process. Due to this incident, the amount of power dissipation of flip-flops in sleep mode and in active mode are same. By the clock network, a significant amount of power is dissipated too. The basic design style separates the whole network responsible for clocking scheme, from the other components of the circuit. We use a different power supply denoted as V(clk) for the circuit responsible for clocking and it is used for measuring clock network dissipated power. Power dissipated by the clock circuit can be seen in Table1. Power dissipation can be saved by disabling the clock network during the sleep mode. The clock network can consume a large portion of power responsible for the system. The implementation of clock gating can disable the clock network from rest of the system.

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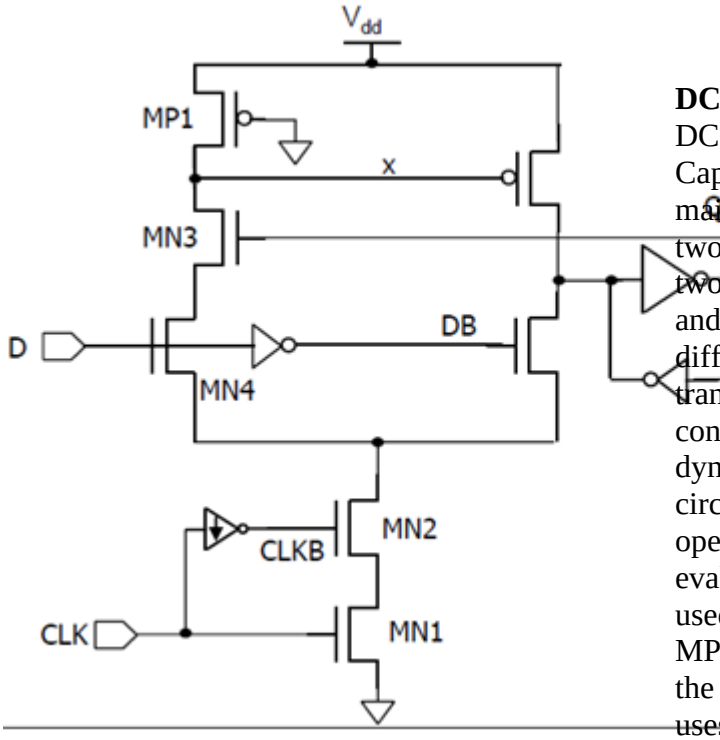

Figure 5.. SCCER flip flop

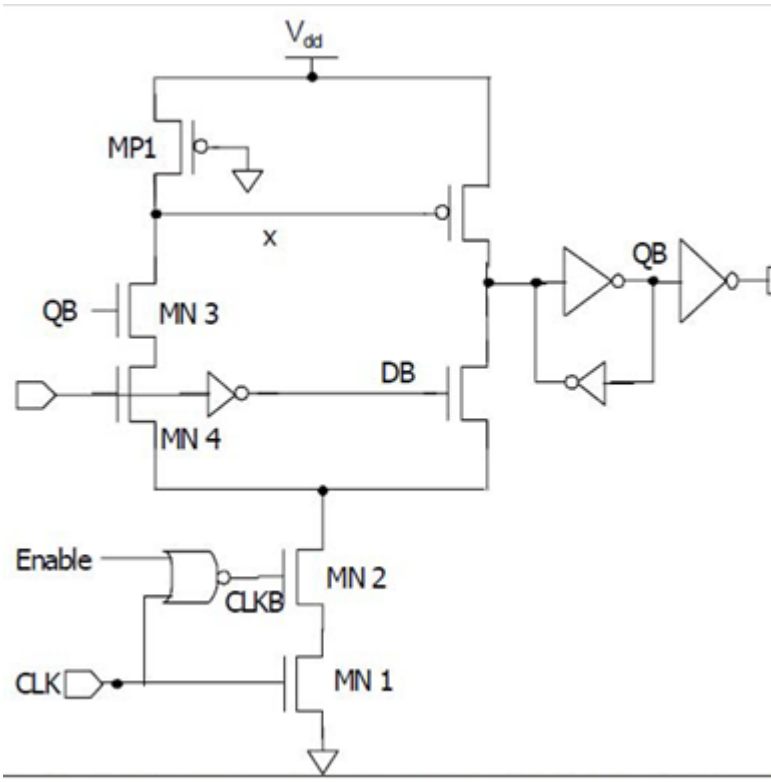

Figure 6. clock gating implemented in SCCER flip-flop

DCCER FLIP-FLOP

DCCER stands for Differential Conditional-Capturing Energy Recovery flip-flop. The main circuit of DCCER flipflop contains two pull up transistors MP1 and MP2 and two pull down transistors MN1 andMN2.The pull down transistors has different names. They are also called control transistors. They provide the necessary control signal to the circuit. Like the dynamic flip-flops of sequential digital circuits, the DCCER flip-flop has their operative mode namely precharge and evaluation. In precharge phase clock is not used but small pull-up PMOS transistors MP1 and MP2 are made operative to charge the prechage node .The DCCER flip-flop uses a latch which is NAND gate based. It operates in Set/Reset latch modes. Here the conditional capturing process is obtained by

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using a feedback path. This feedback path is achieved through the output Q and also through QB and extended to the c transistors MN3 and MN4.These are control transistors and they help to achieve the evaluation paths too.

Generally, in energy recovery logic the clock generator circuit provides the clock continuously even when the input signal is static that means the logical circuit is in idle state.

This incident results a heavy loss of power. Clock gating is an efficient technique to minimize power dissipation in the adiabatic logic circuit. It detaches the clock generator circuit net from the logical net during the idle or non operative periods. Moreover, the clock signal and the distribution network in sequential circuit are the basic contributor to the power dissipation. Moreover, the addition of the clock signal tends to be a heavy load. All of these will add to the capacitance of the clock net.

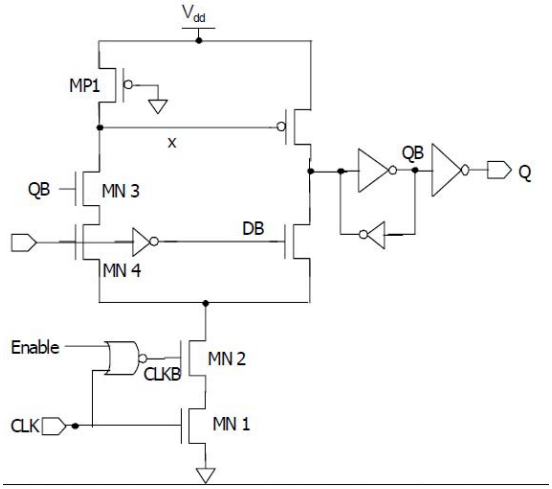

Figure 7. DCCER flip flop

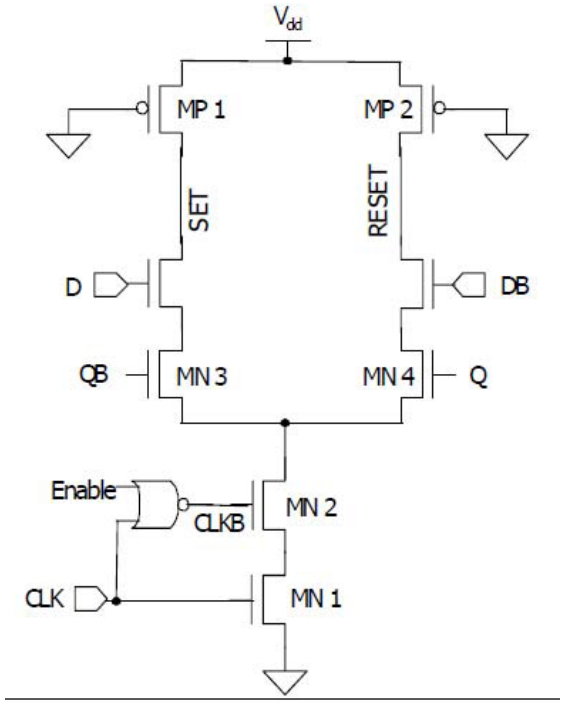

Figure 8. clock gating implemented in DCCER flip-flop

5. RESULT

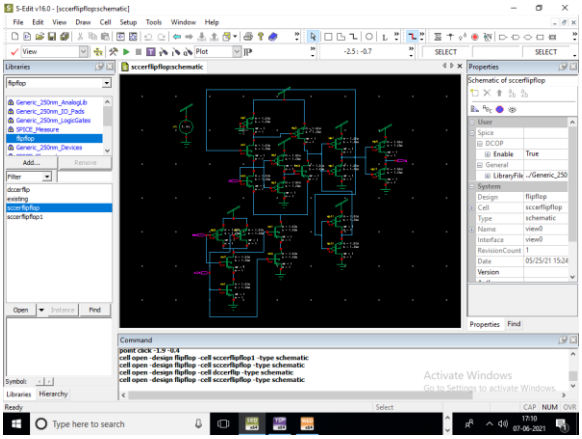

Fig 9 Circuit connection of dccer flip-flop u

The above figure represents the circuit of master- slave D-flip-flop

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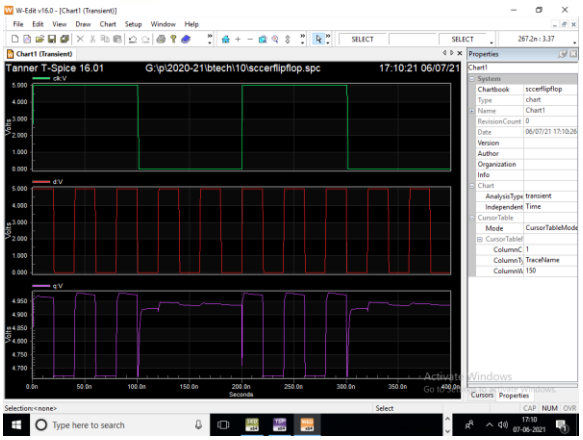

Fig10 Simulation wave forms

The above circuit represents the outputs wave forms of the low power 19- transistor true single phase clocking using reduction schemes,v(clk) is the clock input of the citcuit, v(d) is the data input of the circuit, v(q), is the output of circuit.

6.CONCLUSIN

We present a novel FF design achieved by employing a modified SR latch structure incorporating a hybrid logic consisting of static-CMOS logic and CPL. The key idea is providing an additional discharge path between the master and slave latches, which not only shortens the transition time to enhance the power and speed performance, but also reduces circuit complexity for better timing parameters. Extensive simulations were conducted and various performance indices such as power consumption, PDP, setup time delay, and CQ delays were evaluated. The proposed design was determined to excel in almost every performance index, except for hold time performance. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design.

We hope that presented results will encourage further research activities in TCFF technique. The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility. More work was recently done in automation of logic design methodology based on TCFF technology.

7.FUTURE SCOPE

In the future system design the transistor count is further reduced from 19 to 18. This reduction simplifies the circuit and the power consumption also reduced. Figure 3 shows the structure of 18 transistor FF design. In this design the transistor in the master latch is combined with the clock signal and thus the transistor count is reduced by one.

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