International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

DESIGN A SELF REPAIRABLE FAULT TOLERANT SYSTEM USING PCG

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ABSTRACT:
In this paper, design a self repairable fault tolerant system using PCG (Preconditioned Conjugate Gradient) is implemented. Basically, multiplexers are key arithmetic circuits in many of these applications including digital signal processing (DSP). Initially here input is given to the flip flop block and shadow latch block. The flip flop will save the input data into two states as '0' and '1'. Shadow latch will also save the input data but it will capture the input data and present it on the data line. Flip flop will transfer the input data to perform the main operation and shadow latch will save the data in shadow memory. At last the both data will be compared using comparator and output is obtained. Hence this paper reduces the errors, delay and area in effective way compared to earlier systems.

KEY WORDS: VLSI, Digital signal processing (DSP), Multiplexer, Fault tolerant system, self repairable, PCG (Preconditioned Conjugate Gradient), Comparator.

I.INTRODUCTION

One of the most pressing hurdles in the development of innovative computation paradigm is energy dissipation. In recent years, reversible logic is a promising computing paradigm having application in low power CMOS, quantum computing, nanotechnology and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. The main advantage of this technology is, it minimize the amount of energy dissipation. Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generates kBTln2 joules of heat energy, where kB is Boltzmann's constant and T is the absolute temperature at which computation is performed.

Another scientist Bennett showed that kBTln2 energy dissipation would not occur, if a computation is carried out in a reversible way. Reversible circuits are those circuits that do not lose information. The amount of energy dissipation directly depends on the number of bits lost. It has been shown that reversible logic helps in saving energy using charge recovery process. Reversible computation in a system can be performed only when the system comprises of reversible gates.

To get high speed the critical path should be as minimum as possible. Similarly to get low power less number of gates are used at circuit level without compromising the accuracy of the circuit. Multiplexers are used in wide variety of applications like adders, multipliers, communication, digital signal processing etc. Based on the selection signal multiplexer will select the input data and passes it to the output. The presence of fault in a multiplexer cause's invalid data at the output. The multiplexer should be fault

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secure so that it gives valid data at the output even though faults are present in it.

Two clocking schemes, namely Landauer clocking and Bennett clocking, are analysed for energy dissipation and performance analysis of QCA systems. One of the main objectives of emerging computational technique is power dissipation. Researchers like Landauer have shown that irreversible logic computation generates kBTln2 joules of heat energy for each bit of information loss, where kB is Boltzmann constant and T is the absolute temperature at which computation is performed.

Bennett showed that kBTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [9], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Landauer clocking is simple but it makes some devices such as the Majority Voter to be irreversible and dissipative. Bennett clocking is used for higher throughput and low power dissipation and it has been proposed for reversible computing in QCA. Reversible circuits are those circuits that do not lose information and dissipate very less heat.

Thus, reversible logic is likely to be in demand in high speed and low power computing. There are two types of Reversible Logic; Thermodynamic and Logic reversibility. Thermodynamic reversibility of a computing system refers to zero-energy dissipation such that the internal structure of the system must satisfy strict reversible primitives in a given technology implementation. Note that thermodynamic reversibility requires logic reversibility; however, a circuit can be logically reversible, but not thermodynamically reversible.

Self checking multiplexer was introduced. This self checking multiplexer designed by using four transmission gates and an inverter as shown in Fig. 1. When CS is low S0N is passed to SN. Similarly when CS is high S1N is passed to SN. Thus it implements the function of multiplexer. In this self checking multiplexer when SN and SN_bar are same then it shows the presence of a fault. By using this structure only fault is detected and can't be repairable. To make the multiplexer self repairing two different structures are proposed. The CS bar signal is the inverted signal of CS.

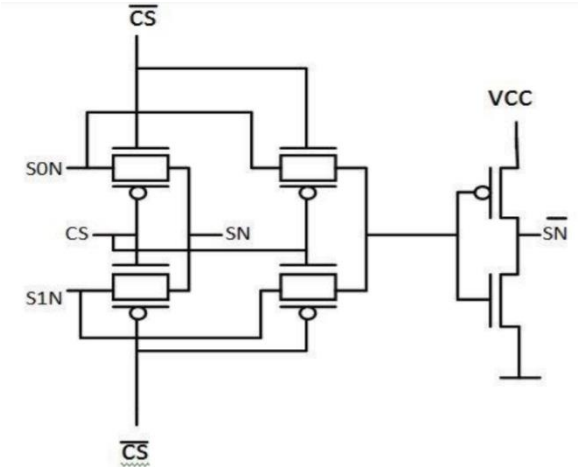

Fig. 1: SELF CHECKING MULTIPLEXER

II. REAL-TIME SELF REPAIRABLE MULTIPLEXER FOR FAULT TOLERANT SYSTEMS

This section describes the proposed self repairing multiplexer1 which uses additional circuitry to detect and repair fault. The circuit diagram is shown in Fig. 2.

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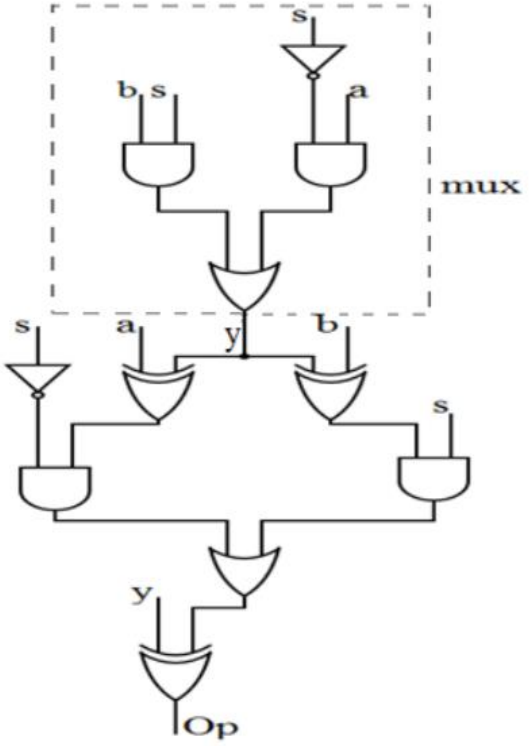

Fig. 2: SELF REPAIRING MULTIPLEXER 1

In Fig. 2 the circuit enclosed in square box shows the basic structure of 2:1 multiplexer. Remaining structure which is not included in the square box is used for repairing the above 2:1 multiplexer. The circuit is able to detect all possible single and multiple faults present in the 2:1 multiplexer and repairs the circuit. The circuit gives 100% error recovery. Consider Fig. 2.

Assume there is a stuck at '0' fault at y. Since y was stuck at '0', it will give always '0' as the output. However when this value is passed to repairing circuit, it detects the fault and produces correct output. This is shown in Fig. 6. Similarly assume there is a stuck at '1' fault at y. Since y was stuck at '1', it will give always '1' as the output. However when this value is passed to repairing circuit, it detects the fault and produces correct output.

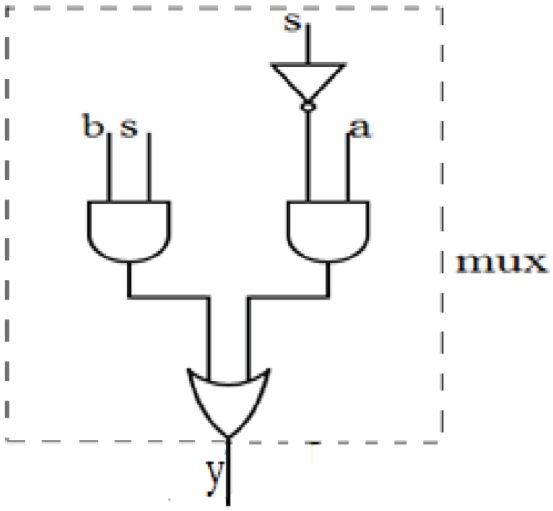

Fig. 3: SELF REPAIRING MULTIPLEXER 2

This is shown in Fig. 3. So when there is fault in multiplexer block, then output Op gives the inverted value of y. If there is no fault, then y value is passed to the output Op. The above proposed multiplexer 1 uses additional circuitry to repair. In the proposed self repairing multiplexer 2 the building blocks of multiplexer itself are self repairable.

III. SELF REPAIRABLE FAULT TOLERANT SYSTEM USING PCG

The below figure (4) shows the block diagram of proposed system. Initially here input is given to the flip flop block and shadow latch block. The flip flop will save the input data into two states as '0' and '1'. Shadow latch will also save the input data but it will capture the input data and present it on the data line. Flip flop will transfer the input data to perform the main operation and shadow latch will save the data in shadow memory. At last the both data will be compared using comparator and output is obtained

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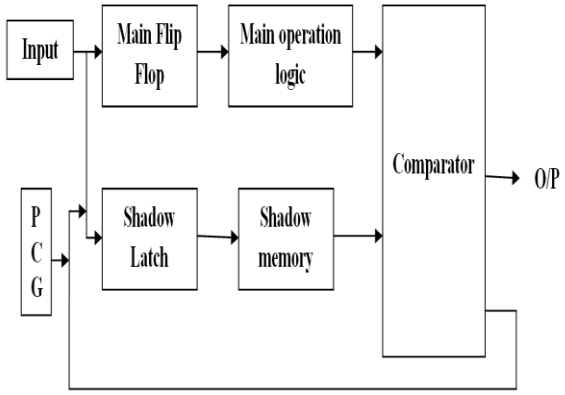

Fig. 4: BLOCK DIAGRAM PROPOSED SYSTEM

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals and and one binary digital output. A comparator circuit compares two voltages and outputs either a 1 (the voltage at the plus side; VDD in the illustration) or a 0 (the voltage at the negative side) to indicate which is larger. Comparators are often used, for example, to check whether an input has reached some predetermined value.

Shadow latches are a kind of latch, sometimes out of synchronization with the other latches, sometimes software based, sometimes hardware configured. You will find this kind of circuit design in high speed digital signal processing applications. A latch circuit allows all the various connected circuits to stabilize in a state, it essentially acts as a control mechanism to assure states are captured if other elements of the design are faster or slower. Shadow latches are a kind of latch, sometimes out of synchronization with the other latches, sometimes software based, sometimes hardware configured.

A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics. Flip-flops and latches are used as data storage elements. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either level-triggered (asynchronous, transparent or opaque) or edge-triggered (synchronous, or clocked). The term flip-flop has historically referred generically to both level-triggered and edge-triggered circuits that store a single bit of data using gates. Recently, some authors reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called transparent latches. Using this terminology, a level-sensitive flip-flop is called a transparent latch, whereas an edge-triggered flip-flop is simply called a flip-flop. Using either terminology, the term "flip-flop" refers to a device that stores a single bit of data, but the term "latch" may also refer to a device that stores any number of bits of data using a single trigger. The terms "edge-triggered", and "level-triggered" may be used to avoid ambiguity.

IV. RESULTS

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The below figure (5) the RTL schematic of proposed system.

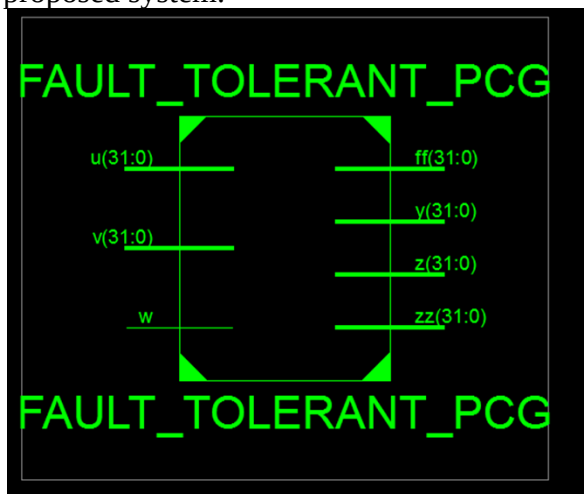

Fig. 4: RTL SCHEMATIC OF PROPOSED SYSTEM

The below figure (5) shows the Technology schematic of proposed system.

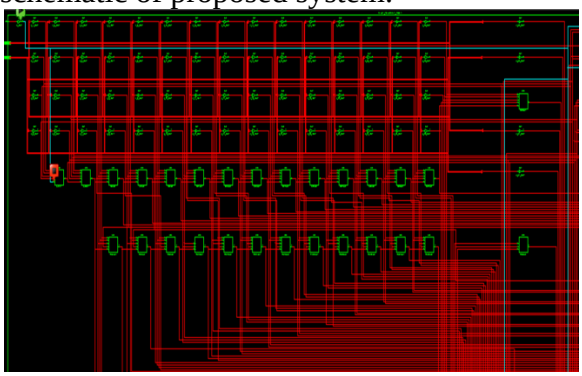

Fig. 5: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM

The below figure (6) shows the output waveform of proposed system. The entire project is implemented using 64 bits.

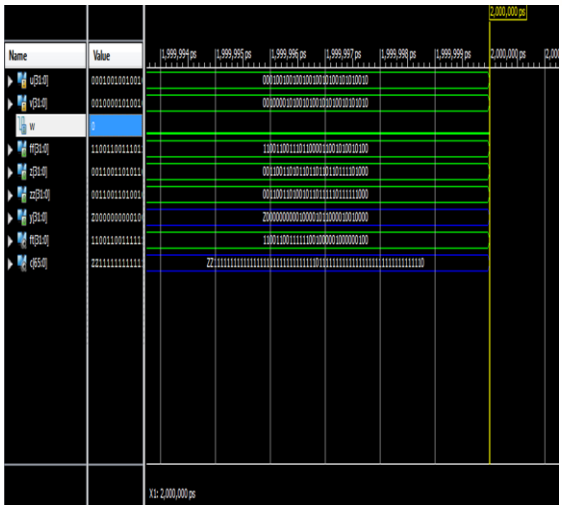

Fig. 6: OUTPUT WAVEFORM OF PROPOSED SYSTEM

V. CONCLUSION

Hence, in this paper design a self repairable fault tolerant system using PCG (Preconditioned Conjugate Gradient) is implemented. Basically, multiplexers are key arithmetic circuits in many of these applications including digital signal processing (DSP). Initially here input is given to the flip flop block and shadow latch block. Hence this project reduces the errors, delay and area in effective way compared to earlier systems.

VI.REFERENCES

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