International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

IMPLEMENTATION OF HYBRID FULLADDER

Dr. G. PADMA PRIYA[1], PARUSU MEGHANA[2],RACHAMALLA SIREESHA[3],MANKUSAHITHI[4],P VS VIKAS[5], PERINATINAVEEN[6]

[1]AssociateProfessor,Dept.ofECE,SVCollegeofEngineering,Tirupati,A.P,India.

[23456]B.TechStudents,Dept.ofECE,SVCollegeofEngineering,Tirupati,A.P,India.

ABSTRACT

Adder plays an important role in the design of FIR filters in digital signal processors(DSP).InVLSItheadder'sperformancespeedaffectstheoverallspeedofthesystem.Moreover ,Multiplication processusesexecutiontimeinmostoftheDSPdevices. Hence, high speed is required in multiplier. This paper presents the analysisof a high-speed new adder using Shannon adder.The proposed hybrid adder isimplemented in order to achieve higher reduction of power. The circuit simulationsare done using Tanner EDA software. The obtained simulation results exhibit thatthe proposed structure performance is better in terms of Propagation delay, lowpower consumption and Power delay product when compared with the advancedtechnologyin CMOS.

Keywords-Shannonadder,hybrid fulladder,Powerdelay product

.

INTRODUCTION

Now Days, portable electronic gadgets, such as cellular phones, personal digitalassistants, and notebook, form the integral part of life. For harnessing best out ofthese electronic systems, designers strive for small size, high speed, and energy-efficient circuits. These electronic systems mostly comprise arithmetic circuits. An adder is a fundamental component of most of the arithmetic circuits such as multipliers. These arithmetic circuits are extensively used in the datapaths consuming almost one-third of power in the high-performance microprocessors. The important process in VLSI circuit design is in reducing the area and designingwith low power consumption. Addition also is an important operation of ALU ofALU operations like

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

division, multiplication and Subtraction. For example, fulladdercellsandthehalfadderce lls,areusedtocompletethemultipl icationalgorithm.

An adder is a digital circuit that performs addition of numbers. In many computersand other kinds of processors adders are used in the arithmetic logic units or ALU.They are also used in other parts of the processor, where they are used to calculateaddresses, table indice, increment and decrement operators and similar operations.Although adders can be constructed for many number representations, such asbinary-coded decimal or excess-3, the most common adders operate on binarynumbers. In cases where two's complement or ones' complement is being used torepresentnegativenumbers,itis trivialtomodifyanadderintoanad der–subtractor.

LITERATUREREVIEWOFFULLADDER

The circuit diagram of a 3-bit full adder is shown in the figure. The output of XORgateiscalledSUM,whiletheo utputoftheANDgateistheCARRY .TheANDgateproducesahighoutp utonlywhenbothinputsarehigh.Th eXORgateproduces a high output if either input, but not both, is high. The truth table of 3-bitfull adder is given. The 3-bit full adder circuit has a provision to add the carrygeneratedfrom thelower bits.

TheexpressionforSUMandCARRYisgivenby,

$$SUM=A \oplus B \oplus Cin$$

$$CARRY=AB+Cin(A \oplus B)$$

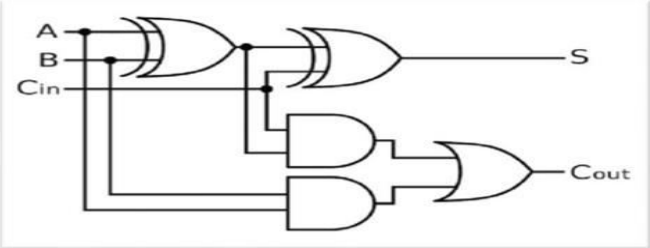

Fig1.FullAdderCircuit

Table1:FullAdderTruthTable

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

EXISTINGMETHOD

Inthisarticle,anewXOR–XNORcircuitisproposed,whichprovidesgooddrivingcapabilitiesandfullswingXOR–XNORoutputswithoutusinganyexternalinverter.Inthisdesign,afeedbackcircuitryandinternalNOTgatehelpingettingfullswingoutputforallthetransitions.UsingtheproposedXOR–XNOR circuit, four different designs of FA are also presented in this article.The proposed FA show improvement in terms of power delay product (PDP) anddrivingcapabilitythanthoseofotherstructures.

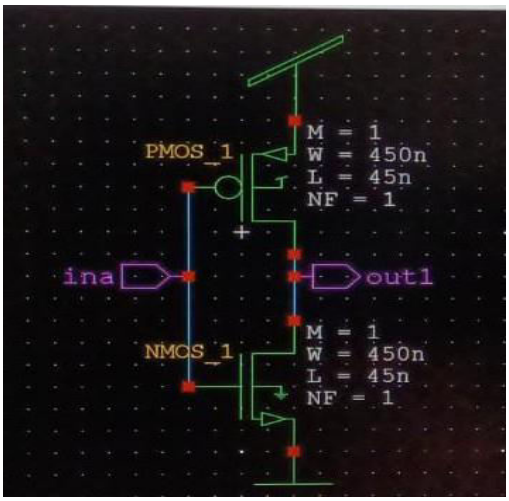

Fig2:Pass Transistor

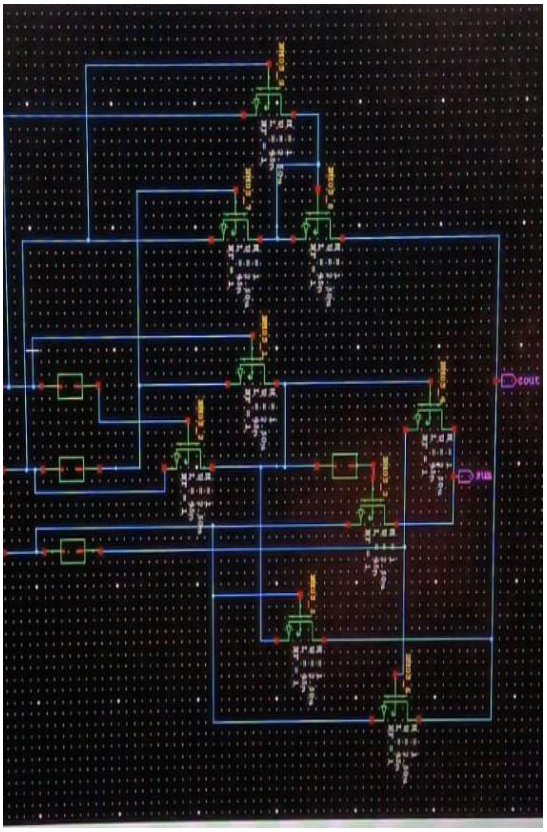

Fig3:ShannonFullAdder

PROPOSEDMETHOD

Multiplier plays an important role in the design of FIR filters in digital signalprocessors (DSP). In VLSI the multipliers performance speed affects the overallspeed of the system. Moreover, multiplication process uses execution time in mostoftheDSPdevices.Hence,highspeedisrequiredinmultiplier.Thispaperpresentstheanalysisofahigh-speednewadderusingShannonadd

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

er.Theproposed hybrid adder is implemented in order to achieve higher reduction ofpower.

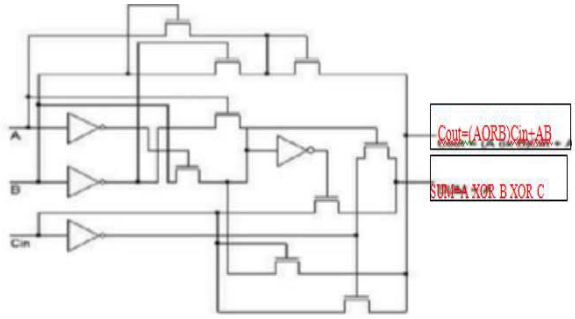

Fig4:ShannonFullAdder

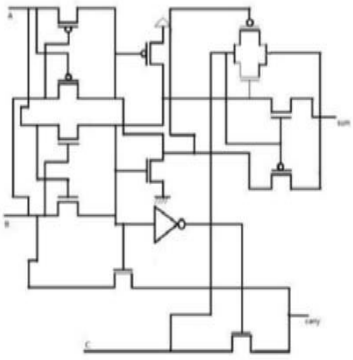

Fig5:HybridFull Adder

METHODSORTECHNIQUESUSEDINOUR PROJECT

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allowyou to enter. schematics, perform SPICE simulations, do physical design (i.e., chiplayout), and perform design rule. checks (DRC) and layout versus schematic (LVS)checks.

SIMULATIONRESULT

The design cycle for the development of electronic circuits includes an importantpre-fabricationverificationphase.Because oftheexpenseandtimepressuresassociatedwiththefabricationstep,accurateverificationiscrucialtoefficientdesign. The role of EDA tool is to help design and verify a circuit's operation bynumericallysolvingthedifferentialequationsdescribingthecircuit. Thesesimulationresultsallowcircuitdesignerstoverifyandfine-tunedesignsbeforesubmittingthem for fabrication.

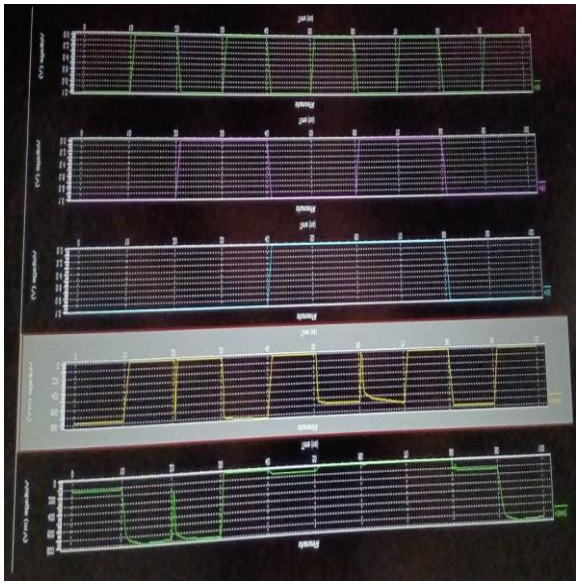

Fig 6: Output Waveforms of Shannon Full Adder

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

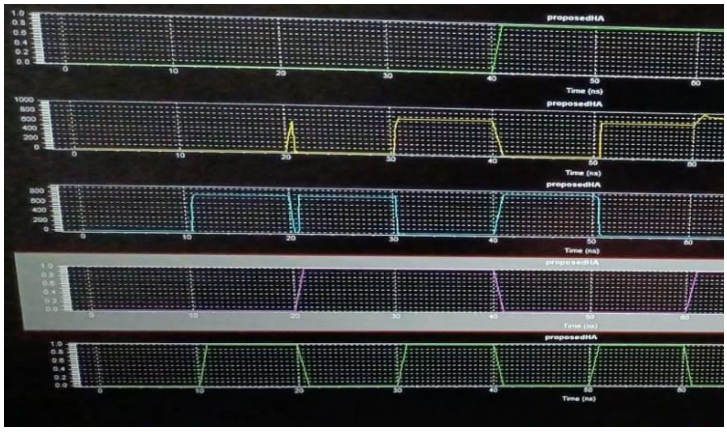

Fig 7: Output Waveform of Hybrid Full Adder

Table2:SimulationResult

S.No	Parameter	ShannonFull Adder
1.	AveragePower	7.853185e-005 W
2.	Time	0to1e-007

CONCLUSION

Transient analysis is performed in order to evaluate the performance of proposedhybrid full adder, hybrid adder and Shannon adder, circuits. This paper discusses onthecircuitsbasedontheproposed hybridadderandexistingadderwhi charedesigned using 45nm CMOS based Technology. T-Spice simulation tool is used forperformingthe required simulations.

FUTURESCOPE

In future, we are extending our design by implementing an applications such asALU, Multipliers and Ripple Carry Adders. And also we can apply any type oflowpower techniques for further power reduction and fast performance.

REFERENCES

1. BhavyaLahariGundapaneni and JRK Kumar Dabbakuti "Booth Algorithm fortheDesignofMultiplier"-InternationalJournalofInnovativeTechnologyandExploring Engineering.
2. D.ChandrikaSowmini"InternationalJournalofInnovative TechnologyandExploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9, Issue-2, December-2019.
3. International Journal of Recent T rends in Engineering & Research(IJRTER)Conference on Electronics, Information and

Communication Systems(CELICS'18)SpecialIssue;March-2018[ISSN:2455-1457]DOI:10.238883/IJRTERCONF.02180328.031.MFPRK.

4.MarianoAguirre-HernandezandMonicoLinares-"ArithmeticApplications"IEEETRANSACTIONSONVERYLARGESCALEINTEGRATION(VLSI)SYSTEMS,VOL 19,NO-4,PP.718-721,APRIL-2019.

5.PygastiJuveria and K.Ragini - "Low Power and High Speed Full Adder usingnew XOR and Xnor Gates" International Journal of Innovative Technology andExploringEngineering (IJITEE)ISSN : 2278-3075,Volume-8 Issue-8 June-2019.

6.RidhiGarg"ReviewpaperofModifiedBoothMultiplierwithDifferent Methods"InternationalJournalofEngineeringDevelopmentandResearch 2018|Volume 6, Issue 2| ISSN: 2321-9939.

7.SupriyaS.Saste and Prof.Anil ;G.Sawant"Design and Implementation of Radix 4BasedMultiplicationonFPGA"InternationalJournalof EngineeringResearch&Technology (IJERT) ISSN : 2278-0181 VOL.5 Issue 09, September-2016.8.Sathiyabama.

8.G.,Malarkkan.S.,"DynamicPowerReductioninCarrySaveMultipliers using Multi VDD Technique with Single Supply Level Converter",2012.9.Oscal.T ,Chen.C,Wang.S,andYW Wu,"MinimizationofSwitchingActivitiesofPartialProductsforDesigningLow-PowerMultipliers,IEEETransactiononVeryLarge Scale Integration(VLSI)Systems,

2008; 11(3),pp. 418-33.

9. Shigeharu,KenjiOka"AutomatedLicensePlateDetectionusingaSupportVectorMachine "2016.
10. Shivani Sharma, GauravSoni, "Comparative study of fin FET based 1-bit full adder cellimplemented using TG And CMOS logic styles at 10, 22 And 32nm", IOSR Journal of VLSI andSignalProcessing(IOSR-JVSP),Volume6, Issue 1,Ver. I(Jan.-Feb.2016).
11. S.M.KangandY.Leblebici ,"CMOSdigitalintegrated circuitsanalysisanddesign ",McGraw-Hill,New York,USA-2003.