International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

An Efficient Performance of Image Scaling Based VLSI Architecture for Multimedia Applications

Kampasati Sateesh, M.Tech Scholar,Dept of ECE, NNRESGI.
Koustubh Kulkarni, Assistant Professor,Dept of ECE, NNRESGI.
Aare.Gopal, Associate Professor,Dept of ECE, NNRESGI.

ABSTRACT

Image scaling refers to the resizing of an image and is done quite often during DigitalImage Processing. In this paper, an efficient image scaling algorithm and its architecture isdeveloped which produce good quality resized image with lesser area and high performance. Ituses a linear space-variant edge detector for edge enhancement and a spatial sharp filter forreducing the blurring effects produced by the bilinear interpolation. A simplified bilinearinterpolation is used which is hardware efficient. The existing algorithms are implemented in Matlab and the Proposed model Implemented in Xilinx.

INTRODUCTION

Image scaling is a time-consuming operation that necessitates a trade-off between efficiency, smoothness, and sharpness, among other considerations. As the number of visual and video applications for mobile cell devices continues to rise, the relevance of picture scaling becomes more apparent. Picture scaling is the process of enlarging or shrinking a digital image in computer graphics. Image scaling has been extensively used in the domains of digital imaging devices, and more specifically in the fields of electronic-based imaging devices, for many years. In electronic displays such as digital PDAs, mobile phones, and tablet computers, image scaling is the process of scaling down high - quality frames or photographs to suit tiny size LCD panels on electronic displays. Image scaling techniques may be divided into two types: polynomial-based methods and non-polynomial-based methods. Polynomial-based approaches are the most common. The closest neighbour algorithm is the most straightforward polynomial-based approach available. Although it has the virtue of being simple, the pictures produced as a consequence are cluttered with blocking and aliasing artefacts. The bilinear interpolation technique is the most generally used scaling method because it allows the target pixel to be achieved by applying linear interpolation in both the horizontal and

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

vertical axes. The bilinear interpolation algorithm is based on the linear interpolation algorithm. Another prominent polynomial-based approach is the bi-cubic interpolation algorithm, which employs an upgraded cubic model to get the resulting pixel by means of a 2-D regular grid and then divides the resultant pixel by the number of pixels in the grid. In addition, a large number of high-quality non-polynomial-based approaches have been suggested.

These unique approaches will increase picture quality by the use of several efficient techniques such as curvature interpolation, bilateral filter, and autoregressive model, among other things. These strategies effectively increase the picture quality while also reducing the artefacts caused by the blocking, aliasing, and blurring effects on the image. However, these high-quality picture scaling methods have a high level of complexity as well as a large memory need, making them difficult to implement in a VLSI device. Image processing algorithms with minimal complexity and low memory requirements are thus required for VLSI implementation in real-time applications with low memory requirements and high throughput. Some earlier research have provided low-complexity VLSI implementation approaches for real-time picture scaling applications, which can be implemented using VLSI. These are the area-pixel model Winscale and an efficient VLSI design, an area-pixel-based scalar design advanced by an edge-oriented technique, a Real-time FPGA architecture of extended linear convolution for digital image scaling, an efficient VLSI design of bi-cubic convolution interpolation for digital image processing, and an area-pixel-based scalar design advanced by an edge-oriented technique. This is an adaptive scalar with great quality at a cheap cost that may be used in real-time multimedia applications. Previous work developed an adaptable real-time, low-cost, and high-performance picture scalar based on four line buffers that could be used in any situation. An adaptive strategy based on the bilinear interpolation algorithm is used to enhance the picture quality by adding sharpening spatial and clamp filters as pre-filters and by using a sharpening spatial and clamp filter as pre-filters.

Literature survey

It still needs four line buffers, despite the fact that the memory demand and hardware cost have been significantly lowered by efficient design. As a result, in this paper, a low-cost, low-area, low-

memory-requirement, and efficient image scalar architecture is provided for implementation.

1. A low-cost high-quality adaptive scalar for real-time multimedia applications

It is shown in this research that an unique adaptive scaling method may be utilised to construct a VLSI scaling circuit that is cheap in cost, low in power, and high in performance for picture zooming applications. Because of its low complexity and great quality, bilinear interpolation has been chosen as the interpolation technique of choice. The use of a clamp filter and a sharpening spatial filter as pre-filters is intended to mitigate the deficiencies of blurring and aliasing effects induced by the bilinear interpolation algorithm's shortcomings. The quality of the scaled pictures produced is noticeably enhanced when adaptive skill is used in conjunction with it.

2. Curvature Interpolation Method for Image Zooming

This approach, known as the curvature interpolation method (CIM), makes use of a unique interpolation algorithm that is successful in picture zooming while also being simple to apply. It is possible to split the new approach into three steps: determining the curvature from an existing LR picture, calculating the interpolation of the curvature, and creating the zoomed image by solving the curvature equation algebraically. In order to decrease interpolation artefacts, the CIM develops the generated picture by using the interpolated curvature as a driving force, rather than directly interpolating the image itself, as opposed to direct interpolation of the image.

3.VLSI implementation of an edge oriented image scaling processor

Image scaling is a highly common approach that has been extensively employed in a broad variety of digital imaging applications for quite some time now. An area-pixel scaling processor with an emphasis on the edges is presented in this study. In order to achieve cheap cost, the area-pixel scaling approach is implemented in the design using a VLSI architecture with a low level of complexity. A basic edge capturing approach is incorporated in order to successfully increase the picture edge characteristics in order to get higher image quality overall. It is anticipated that this effort will result in a processing rate of 200 megapixels per second for a clock period of 5 nanoseconds. The architecture is dependable while dealing with both monochrome and colour photographs.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Proposed model block diagram

Figure 1 is a block diagram of the suggested picture scaling method, which is described in detail below. The clamp filter and sharpening filters are placed in front of bilinear interpolation as pre-filters in order to decrease the noises caused by bilinear interpolation, such as blurring and aliasing artefacts, and to improve the overall quality of the image. This spatial filter is used to enhance edges and reduce related noise, whereas a clamp filter is used to smooth undesired discontinuous edges of border areas that are present in the image. If the input pixels of the original photos are filtered by a sharpening filter, then the filtered pixels are filtered again by another sharpening filter, then the process may be described as follows: Last but not least, the pixels that have been filtered by both filters are supplied to the bilinear interpolation for up- and down scaling. The spatial and clamp filters are simplified and integrated into a single combined filter in order to save computational resource and memory buffer use.

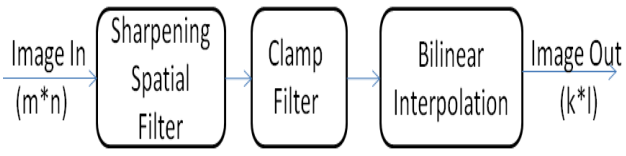


Fig 1. Block diagram of proposed Scaling

Module Description

The filtering and image scaling procedures are dependent on the size of the processing pixel and the size of the convolution kernel. The operations described above may be divided into the following components. A) There is less complication. Sharpening spatial and Clamp filters are used in this application. The sharpening spatial filter is a sort of high pass filter that is used to reduce blurring artefacts in images. It is defined by a kernel and is used to reduce blurring artefacts in images. This technique boosts the luminosity of a core pixel as compared to its surrounding pixels. The clamp filter is a sort of low-pass filter that is often used. It is a 2-D Gaussian spatial domain filter made of a convolution kernel array, and it operates in the spatial domain. It has a single positive value in the centre and is totally rounded to the nearest whole number. This filter is intended to remove aliasing artefacts and smooth the undesired discontinuous edges of the border areas that are present in the image. Clamp filters and sharpening spatial filters are two types of filters that may be represented by convolution kernels. The quality of the photos will improve as the size of the convolution kernel increases. However, a bigger size of convolution filter will need a

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal www.ijarst.in
ISSN: 2457-0362

greater amount of memory and hardware. The memory and processing power required by a 6-by-6 convolution filter, for example, is much more than the two-line-buffer memory and nine arithmetic units required by a 3-by-3 convolution filter, which is substantially smaller.

In the previous work, each of the sharpening spatial and clamp filters was implemented using a 2-D 3 3 convolution kernel to achieve the desired sharpness. In order to run two 3-by-3 convolution filters, at the very least, four lines of buffer memory are required. A cross-model is utilised to replace the 3 3 convolution kernel in order to minimise the complexity of the 3 3 convolution kernel. It was effective in removing four of the nine parameters from the three-dimensional convolution kernel.

Sharpening spatial and clamp filters are implemented using T-shaped and inverse T-shaped model convolution kernels to reduce the VLSI circuit design complexity of the existing cross model convolution kernel. T-shaped and inverse T-shaped model convolution kernels are also used to reduce the VLSI circuit design complexity of the existing cross model convolution kernel. The T-model convolution kernel is formed of the cross-bottom model's four parameters, while the inversed T-shaped model convolution kernel is built of the cross-top model's four parameters, as shown in Figure 1. A combination of T-shaped and inversed T-shaped model filters are used in the proposed picture scaling technique to enhance image quality while concurrently decreasing the size of the images. Thus, the convolution filter's complexity is reduced to an efficient minimum, and the memory need for each convolution filter is reduced from two to one line buffer for each convolution filter. Both models provide convolution kernels for the sharpening spatial and clamp filters to integrate VLSI chip of the proposed low-cost image scaling processor that take up less space, are less sophisticated, and use less memory.

Proposed Pipeline Architecture For Image Scaling

The coupled t-model as well as mirror imaged t-model pooling layer role of a burnishing geographic and indeed the formula was indeed supported such as step 1. Berry. Two. shows its six-stage compute shader architect of something like the blended strainer as well as transfer function one very, that also lessens this same slow direction to enhance this same achievement whilst also process new tech. That whole different phases 1 & 2 through grape. exhibit this same algorithmic

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

planning of both a s n framework merged and also an components t-model separator. A t-model and slightly altered t-model filtration consists of the three and above arithmetic modules (rcus), another multiplier–adder (ma), four different adder circuit (+), thirty subtracters (−), but instead four different switches (s). That whole great opportunity to work of t-model blended separator can just be implement and maintain only with fully connected layers eqs proven to show. It and morals of such eight input pixel value can just be gained as from create an account treasury previously mentioned.

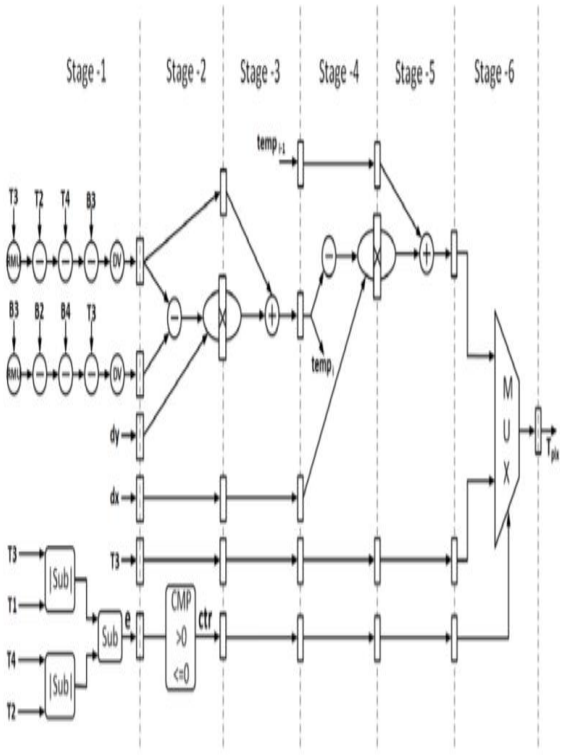


Fig: 2 Proposed Pipeline Architecture For Image Scalar

SYNTHESIS & SIMULATION RESULTS

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	32	4656	0%
Number of Slice Flip Flops	17	9312	0%
Number of 4 input LUTs	55	9312	0%
Number of bonded IOBs	42	232	18%
Number of MULT18X18SIOs	2	20	10%
Number of GCLKs	1	24	4%

Table 1 Device utilization summary for 16-bit

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	21	4656	0%
Number of Slice Flip Flops	9	9312	0%
Number of 4 input LUTs	36	9312	0%
Number of bonded IOBs	22	232	9%
Number of MULT18X18SIOs	2	20	10%
Number of GCLKs	1	24	4%

Table .2 Device utilization summary for 8-bit

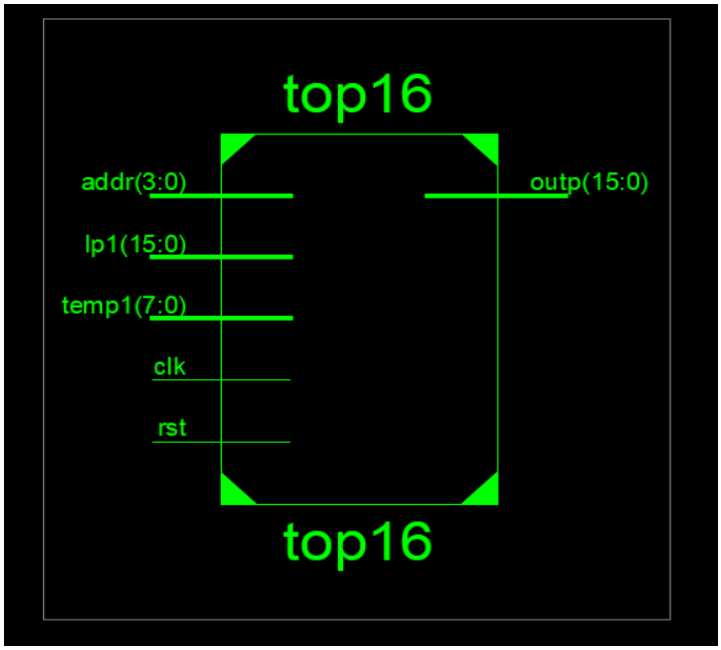


Fig 3 TOP Module

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

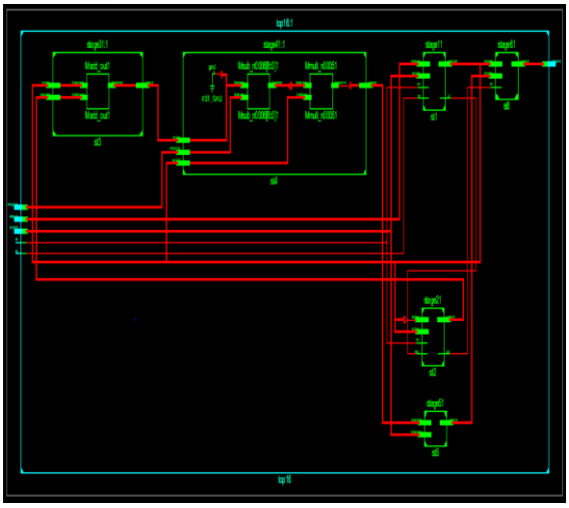
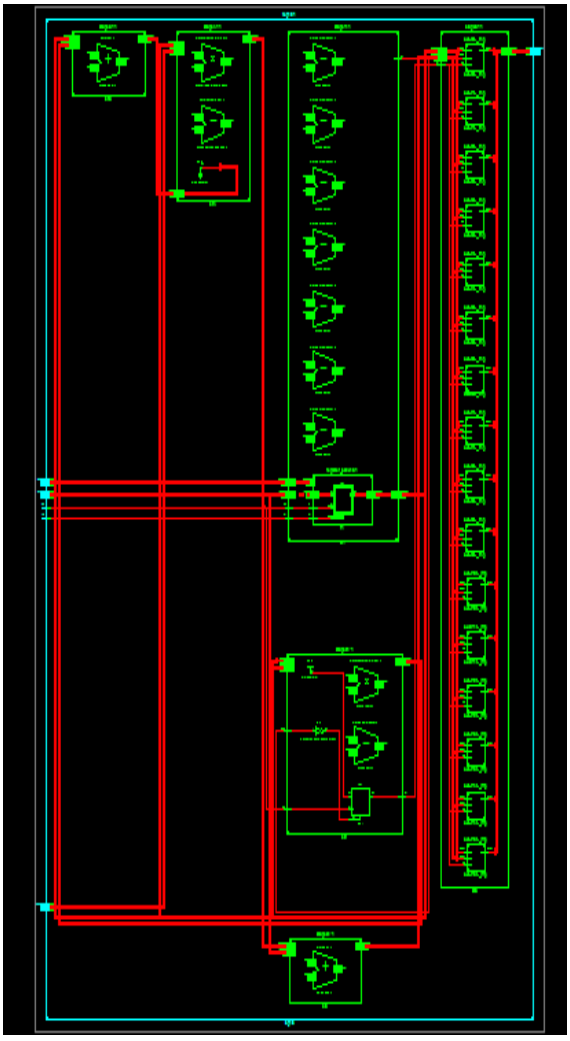


Fig4. RTL Schematic of 16 bit image scaling



t

Fig5. RTL Technological schematic for 16-bit

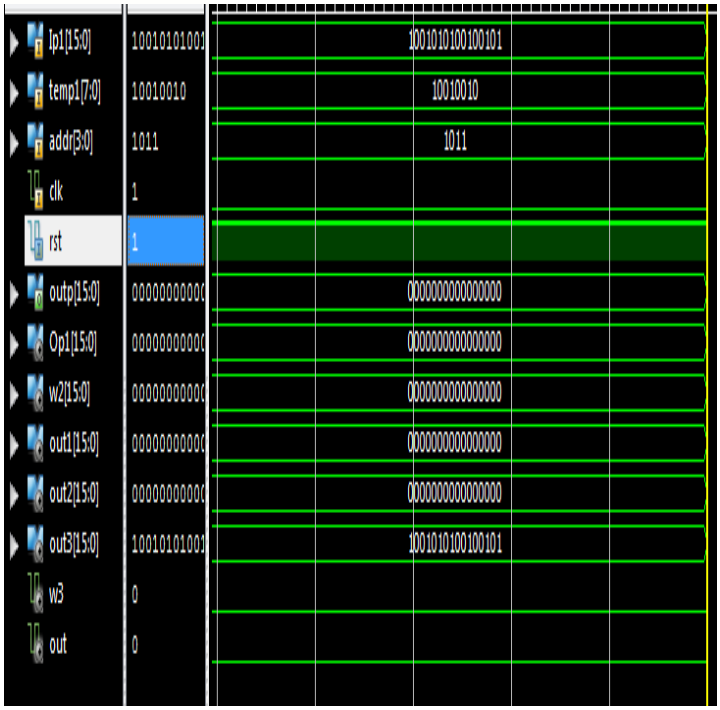


Fig 6(A) simulation results (when reset=1)

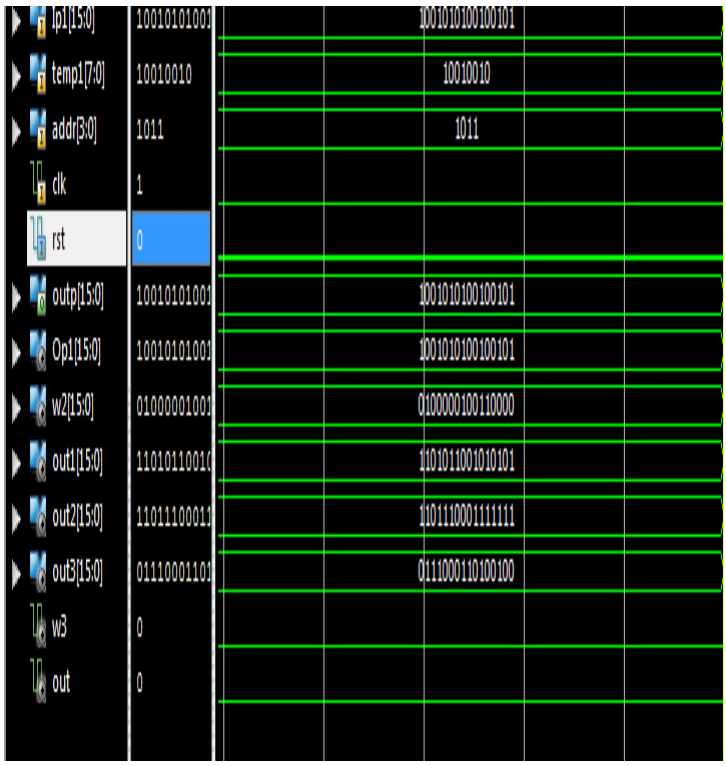


Fig 6(B) simulation results (when reset=0)

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
IJARST
ISSN: 2457-0362

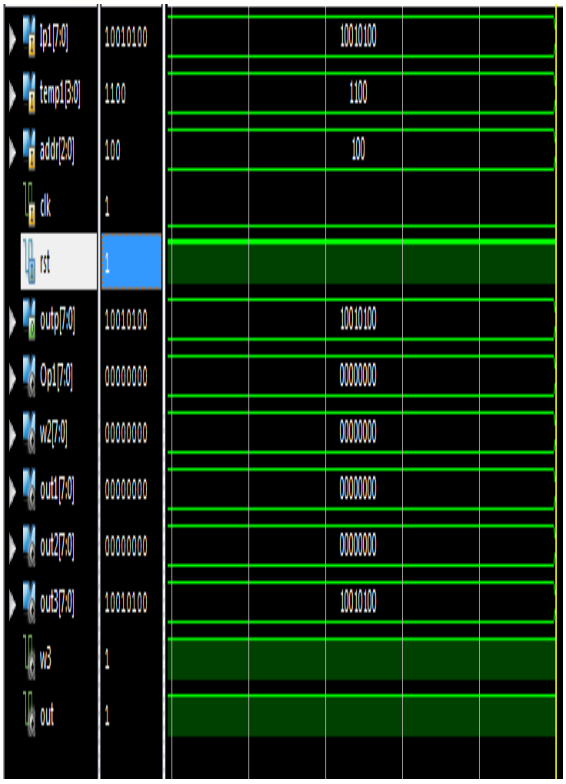


Fig7(A).Simulation results for 8-bit (when reset=1)

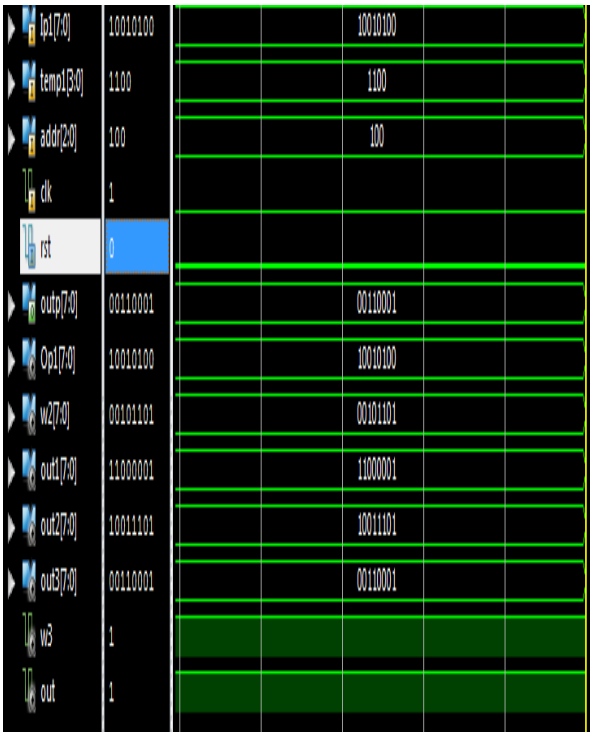


Fig7(B)simulation results for 8-bit (when reset=0)

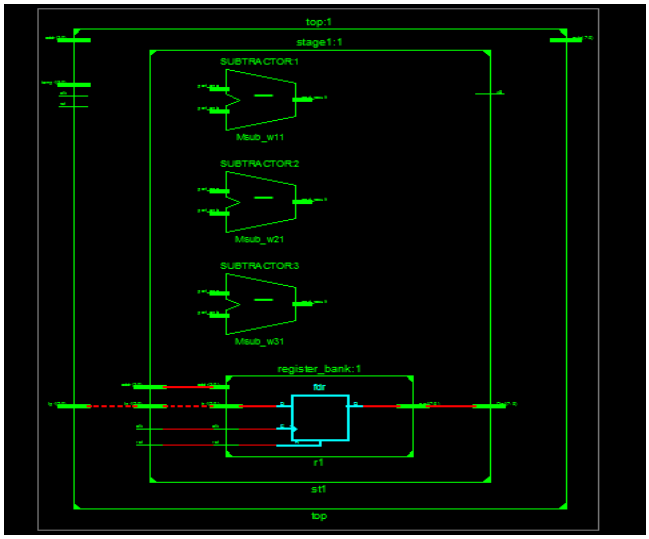


Fig 8: RTL schematic for 8-bit

CONCLUSION

For real-time picture scaling applications, high performance is essential. In this study, we provide a higher-quality picture scalar that is both high-performing and takes up less space. Little-cost edge-catching techniques and a sharp filter with low complexity are used in the suggested design. The bilinear interpolation equation is subjected to algebraic techniques in order to decrease the complexity of the hardware. Based on the adaptive edge enhancement approach, the target pixel is picked as either a bilinear interpolated pixel or the closest pixel to the target pixel.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Device Utilization summary:

Logic Utilization	Total Available	Existing system used (8 bit)	Proposed system used (16 bit)
Number of slices	4656	21	32
Number of flip flops	9312	9	17
Number of 4 input LUTs	9312	36	55
Number of bonded IOBs	232	22	42
Number of MULT18X18SIOs	20	2	2
Number of GCLKs	24	1	1

REFERENCES

[1] H. Kim, Y. Cha, and S. Kim, "Curvature interpolation method for image zooming," IEEE Trans. Image Process. vol. 20, no. 7, pp. 1895–1903, Jul. 2011.

[2] J. W. Han, J. H. Kim, S. H. Cheon, J.O.Kim, and S. J. Ko, "Anovel image interpolation method using the bilateral filter," IEEE Trans. Consum.Electron., vol. 56, no. 1, pp. 175–181, Feb.2010.

[3] X. Zhang and X.Wu, "Image interpolation by adaptive 2-D autoregressive modeling and soft-decision estimation," IEEE Trans. Image Process., vol. 17, no. 6, pp. 887–896, Jun. 2008. [4] F. Cardells-Tormo and J. Arnabat-Benedicto, "Flexible hardware-friendly digital architecture for 2- D separable convolution-based scaling," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 522– 526, Jul. 2006.

[5] S. Ridella, S. Rovetta, and R. Zunino, "IAVQinterval-arithmetic vector quantization for image compression," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. vol. 47, no. 12, pp. 1378– 1390, Dec. 2000.

[6] S. Saponara, L. Fanucci, S. Marsi, G. Ramponi, D. Kammler, and E. M. Witte, "Application-specific instruction-set processor for Retinexlink image and video processing," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 7, pp. 596–600, Jul. 2007.

[7] P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 1, pp. 51–55, Jan. 2009.

[8] M. Fons, F. Fons, and E. Canto, "Fingerprint image processing acceleration through run-time reconfigurable hardware," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 12, pp. 991–995, Dec. 2010.

[9] C. H. Kim, S. M. Seong, J. A. Lee, and L. S. Kim, "Winscale : An image scaling algorithm using an area pixel model,"

IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 6, pp. 549–553, Jun. 2003. R.S. KARTHIC, International Journal of Computer Science and Mobile Computing Vol.2 Issue. 4, April-2013, pg. 46-51 © 2013, IJCSMC All Rights Reserved 51

[10] C. C. Lin, Z. C. Wu, W. K. Tsai, M. H. Sheu, and H. K. Chiang, "The VLSI design of winscale for digital image scaling," in Proc. IEEEInt. Conf. Intell. Inf. Hiding Multimedia Signal Process., Nov. 2007, pp. 511–514.

[11] P. Y. Chen, C. Y. Lien, and C. P. Lu, "VLSI implementation of an edgeoriented image scaling processor," IEEE Trans. Very Large Scale integr.(VLSI)Syst., Vol. 17, no. 9, pp. 1275–1284, Sep. 2009.

[12] C. C. Lin, M. H. Sheu, H. K. Chiang, W. K. Tsai, and Z. C. Wu, "Real-time FPGA architecture of extended linear convolution for digital image scaling," in Proc. IEEE Int. Conf. Field-Program. Technol., 2008, pp. 381–384.

[13] C. C. Lin, M. H. Sheu, H. K. Chiang, C. Liaw, and Z. C. Wu, "The efficient VLSI design of BI-CUBIC convolution interpolation for digital image processing," in Proc. IEEE Int Conf. Circuits Syst., May 2008, pp. 480–483.

[14] S. L. Chen, H. Y. Huang, and C. H. Luo, "A low-cost highquality adaptive scalar for real-time multimedia applications," IEEE Trans. Circuits Syst.Video Technol., vol. 21, no. 11, pp. 1600–1611, Nov. 2011.

[15] K.Jensen and D. Anastassiou, "Subpixel edge localization and the interpolation of still images," IEEE Trans. Image Process., vol. 4, no. 3, pp. 285–295, Mar. 1995.