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LOW RANGE APPLICATIONS FOR SIMULTANEOUS COUNTER USING DIGITAL SWITCHING CIRCUITS

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ABSTRACT: A low-power VLSI circuit is intended to reduce power consumption, increase battery life, and reduce area. The performance of a circuit improves as the circuit's power consumption is reduced. Scaling design or counter is used as a key element for increasing or decreasing the values of an operator depending on its previous state. During the counting process frequency and time can be measured. The major problem in scaling circuit is the power consumption due to the power dissipation in the clock during standby mode. One-third of the total power is consumed by the clock signal in a counter. In this paper, power consumption is reduced by minimizing the number of switching activities. The power consumption in counter further reduced by reducing the power consumption in flip-flops. This can be achieved by combining True Single Phase Clock Logic (TSPCL) with Self-controllable Voltage Level (SVL) technique. TSPCL performs the Flip-Flop operation at high speed with low power. SVL technique suppresses the power due to leakage current and also uses less number of transistors thus the system complexity also gets reduced. The proposed design consumes less power than the existing design. Hence, the proposed methodology reveals promising avenues for low power modern electronics items.

KEYWORDS: Flip-flop, Low power, Scaling circuit, SVL, TSPCL.

I. INTRODUCTION

In today's world, four elements - area, speed, delay, and power consumption – are critical in driving demand for compact handheld devices such as cell phones, laptops, palmtops, and electronic devices. Area, performance, affordability and reliability were formerly the primary considerations of VLSI designers.

In the past, reliability, cost, and performance were prioritised, and power conservation was a minor consideration. However, in recent years, power has been accorded equal weight to area and speed factors. Because of increased frequencies and chip sizes, power consumption has been a critical concern in recent years. Any VLSI circuit's performance is determined by its design architecture, which optimizes power and ensures high reliability. Power optimization of circuits at many levels is required to design any circuit with low power consumption. Power dissipation reduction is a critical design issue in VLSI circuits.

The majority of system-level architectures are made up of sequential circuits, and the design of these circuits has a significant impact on the system's overall power consumption. The clock wastes a lot of electricity in many synchronous applications. The clock is the sole signal that switches continuously, therefore it typically has to drive a vast clock tree. The circuit itself is divided into several blocks. The power dissipation of the clock was lowered in asynchronous applications. Static and dynamic power dissipation contribute the most power to any circuit. Sub threshold conduction, reverse biassedpn junction conduction, gate tunnelling current, drain source punchthrough, gate induce drain leakage, and other factors cause static power dissipation in the quiescent state of the circuit. When compared to dynamic power, however, static power makes a

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small contribution. The transition of signal and short circuit current causes dynamic power dissipation. The transient shorting of the power source and ground during signal transition causes short circuit power dissipation. The contribution of short circuit power to dynamic power is roughly 5–10%.

A Flip-Flop itself a circuit that gives either zero or one as a stable state of the Flip-Flop. It is widely used for storing the information. In sequential logic, Flip-Flop is used as a basic storage element. Scaling circuit is an electronic device that stores the number of times that the process or event has occurred in relation with the clock signal. It is used for counting the number of pulses coming at the input line in a specific time period. The design which consumes lesser power with maximum reliability is almost important especially when it uses clock [6]. Thus, the power of the circuit is minimized by decreasing the dissipation of power in the clock. In Complementary Metal-Oxide Semiconductor VLSI design, the basic classification of counters is synchronous and asynchronous counter and this classification depends on clock triggering. In simultaneous counter common clock is used for all the blocks of Flip-Flop, but in asynchronous counters the output of the previous Flip-Flop can be given as a clock input to the consecutive Flip-Flop. Power efficient with high speed asynchronous ripple scaling circuit uses innovative single edge triggered D Flip-Flop that reduces propagation delay, but it is not suitable for higher operating frequency. Low power scaling circuit based on priority encoding it compresses multiple binary inputs and produces the output from the compressed input. Quasi-synchronous based design optimizes the power dissipation. Toggle scaling circuit [3] based on lesser transition quasi clock. Although these methods which gives the designs in an efficient way but they are restricted by large layout. Bi-stable storage elements are used in low power scaling design [9]. This method has a problem of occupying large space. 1D cellular automation is used in high speed binary scaling circuit [4] whose operation is producing a number sequence that matches the binary number system. It is not suitable for wide range counters. A scaling circuit depends on a diabetic based logic [5] and complementary pass transistor logic is designed. But the adiabatic logic is so complex to design**.** True Single Phase Clock based counter [8], new OR logic is used to implement the counting logic. By reducing the complex and confusing path between the Flip-Flops, the counters operating frequency can be increased. This phenomenon is followed in the TSPC based counter design.

II. LITERATURE SURVEY

Madhu Shakya and Shweta Agrawal, et.al [2] described a recital CMOS D Flip-Flop circuit which is comprehensively used in analog and digital systems. In CMOS technology leakage power is primary significance. To reduce power dissipation and to increase the battery lifetime, the supply voltage should be reduced when the circuit is in off state. Modified SVL technique is applied to CMOS D Flip-Flop circuit, which suppresses the signals and reduces power dissipation because of leakage currents. The consumption of dynamic power is also reduced as minimum number of transistors is used in the modified design.

Raghava Katreepalli and Themistoklis Haniotakis, et.al [1] described a counter is designed which is power efficient due to clock gating. This logic allows the clock switching only when the Flip-Flops are in active state. This technique overcomes the problem of complexity in the circuit. Mozammel HA Khan, et.al [7] proposed “Design of Reversible Synchronous Sequential circuits using Pseudo Reed

Muller expression" and the explained the concept behind the use of Reversible logic and has suggested that sequential circuits be built by replacing the latches and flip-flops and associated combinational gates of the traditional irreversible designs by their reversible counter parts. He has proposed an approach of designing synchronous sequential circuits directly from reversible gates using pseudo Reed–Muller expressions by representing the state transition and the output functions of the circuit. Also, he has presented designs of arbitrary synchronous sequential circuit as well as of counters and registers.

Peiyi Zhao, Jason McNeely, Pradeep Golconda, Magdy A. Bayoumi, Robert A. Barcenas, and WeidongKuang, et.al [10] described the "Low Power Clock Branch Sharing Double Edge Triggered Flip-Flop" technique makes the use of a clock branch-sharing scheme to reduce the number of clocked transistors in the design. The newly proposed design also employs conditional discharge and split-path techniques to reduce switching activity as well as short-circuit currents.

Ahmed Sayed and Hussain Al-Asaad, et.al [11] proposed Cathode Voltage Switch Logic (CVSL) which is conventional switch and inverter based flip-flops, while providing a very stable and easy-to-implement structure, suffer from the lack of flexibility. Extra logic and functionality cannot be easily embedded into such structures. They also consume high power as compared to the other flip-flops. In their study, a new fully-static flip-flop structure is proposed, and compared to the conventional static CMOS flip-flop and the fully-static CVSL flip-flop. An add-and-delay circuit, which is a basic building block for most digital signal processing applications, is designed using this new flip-flop with Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) techniques and compared to a similar circuit implemented.

III. LOW RANGE APPLICATIONS FOR SIMULTANEOUS COUNTER USING DIGITAL SWITCHING CIRCUITS

In this section, discussion of an low range applications for simultaneous counter using digital switching circuits is observed. The design uses the positive edge triggered Flip-Flop. In comparison with the conventional Flip-Flop this TSPCL combined with SVL technique consumes less power.

T or toggle flip flop which is often used for counters can be realized by connecting the J and K inputs of JK flip flop together. All of the popular flip flop can easily be modified to incorporate asynchronous set and/or reset inputs. For master-slave inputs, this normally means adding some extra circuitry to both the master and the slave latch so that the asynchronous inputs will dominate independent of the clock and other inputs. These inputs are often used to initialize the state of digital ICs at the time the power is first applied. Normally, a set or reset input is required, but seldom both. A T flip flop alternately sends an output signal to two different outputs when an input signal is applied.

The design of projected T Flip-Flop design with combined SVL. P1 is ON, N2 is ON, P2, P3 are OFF, N1 and N2 are inactive. In order to perform the normal D Flip-Flop operation, it is connected to supply and GND. When a is inactive, P1, N1, N3 are active and P2, N2 are inactive so that out becomes inactive. When a is 1, which makes P1, N3to inactive state while makes N1, N2 and P2 active state, that is out becomes one.

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Fig. 2: Counter Design using modified Flip-Flop

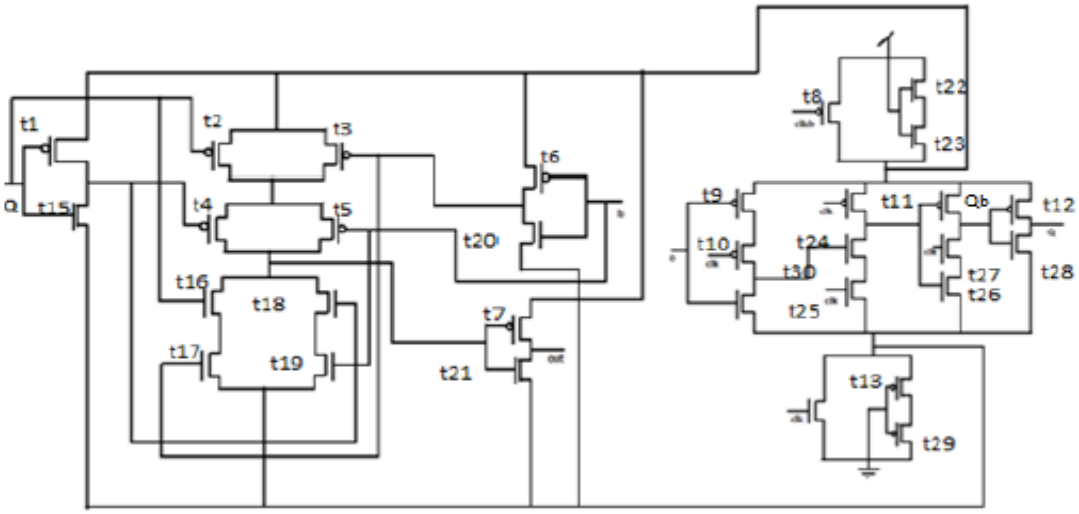
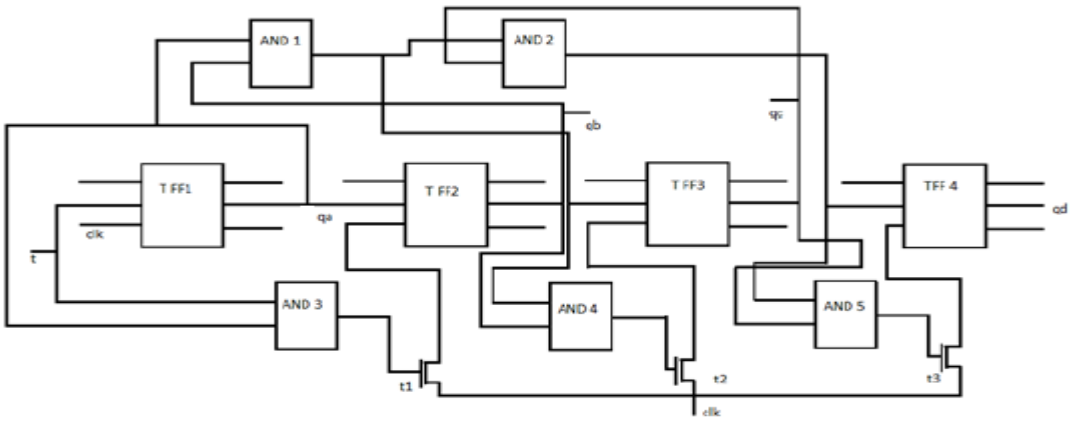


Fig. 1: Design of T Flip-Flop with Combined SVL



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P1, N3 are in OFF state i.e. open circuits. N1, N2 are active but as the supply voltage it gives Vdd-Vth because they acts as a pull-up network. When the NMOS transistors re connected in series it reduces the static power. P2, P3 are active but they gives finite positive voltage as a replacement of GND because they acts as a pull down network. As the NMOS transistors are used in series it reduces supply voltage and also reduces leakage current during standby mode. TSPCL consists of four stages of inverter. The input gets inverted in each stage and the final output of the TSPCL is same as that of the input. The operation of the TSPCL functions according to the clock signal.

A cascade T Flip-Flop structure is used in this system. The reason for using T Flip-Flop is it concerns for the changing activity of next state. It eliminates the clock transition when the input of T Flip-Flop is zero. When the clock is zero it does not affect the output of the circuit and in turn maintains the previous state output whereas the output gets toggled when the clock is one. So, it is evident that the clock acts as a control signal for the counter. The block diagram of proposed counter is shown in Fig. 2.

IV. PERFORMANCE ANALYSIS

In this section performance analysis of an low range applications for simultaneous counter using digital switching circuits is observed.

Table.1: Performance Analysis

Parameters	CVSL	T-flip flop
No. of Transistor	234	162
Power Consumption (μw)	16.67	13.27
Delay (n sec)	266	118

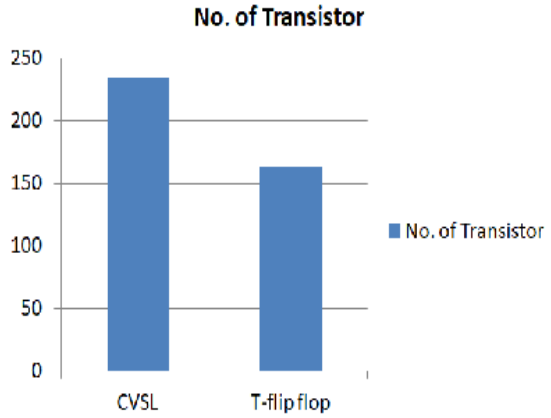

Fig.3: Transistors Comparision Graph

In fig.3 transistors comparision graph is observed between CVSL and T-flip flop. The transistors are less when compared to the other method.

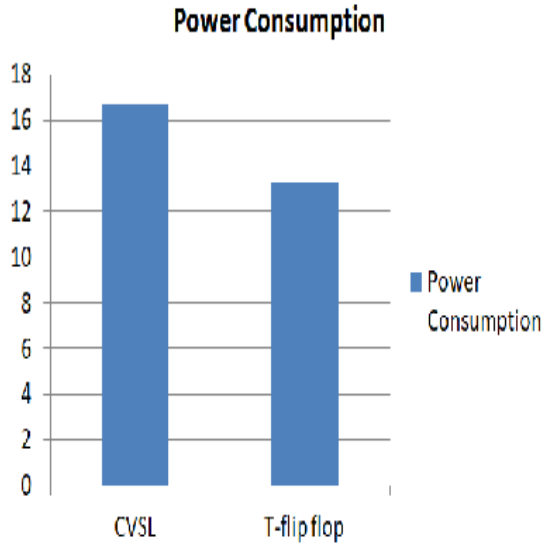

Fig.4: Power Consumption Comparision Graph

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In fig.4 Power Consumption of T-flip flop is lower when compared to the CVSL.

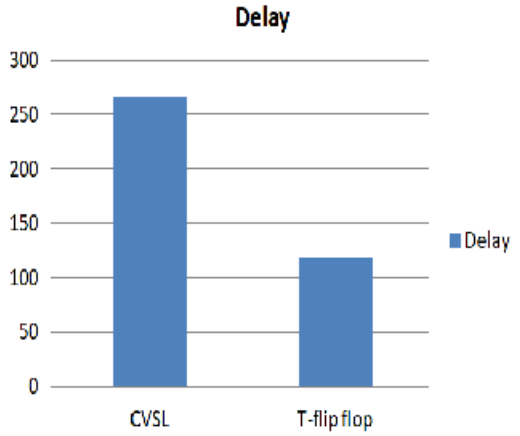

Fig.5: Delay Consumption Comparision Graph

The delay for T-flip flop model is comparatively low with the CVSL.

V. CONCLUSION

The consumption of power in the counter is minimized by using the proposed T Flip-Flop with clock gating technique. The T Flip-Flop is proposed by combining TSPCL and SVL technique. The proposed T Flip-Flop uses only 0.34 microwatt power which is 30% less than the existing T Flip-Flop design. The proposed counter reduces power consumption and chip area which maximizes the battery life and performance of the system.

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